RF POWER AMPLIFIER TECHNIQUES FOR SPECTRAL EFFICIENCY AND SOFTWARE-DEFINED RADIO

Rameswor Shrestha

Graduation committee:

Chairman and Secretary

Prof. dr. ir. A.J. Mouthaan	University of Twente

Promotor

Prof. dr. ir. B. Nauta	University of Twente

Assistant Promotor

Dr. ir. R. van der Zee	University of Twente

Members

Prof. dr. J.R. Long	Technische Universiteit Delft
Prof. dr. ir. A.J.M. van Tuijl	University of Twente
Prof. dr. ir. F.E. van Vliet	University of Twente
Dr. A. Cathelin	STMicroelectronics

Title: RF POWER AMPLIFIER TECHNIQUES FOR SPECTRAL EFFICIENCY AND SOFTWARE-DEFINED RADIO

Author: Rameswor Shrestha

ISBN: 978-90-365-3076-7

ISSN: 1381-3617 (CTIT Ph.D. thesis series No. 10-175)

This work was supported by NXP Semiconductors (former Philips Semiconductors) in Nijmegen, The Netherlands

RF POWER AMPLIFIER TECHNIQUES FOR SPECTRAL EFFICIENCY AND SOFTWARE-DEFINED RADIO

DISSERTATION

to obtain
the degree of doctor at the University of Twente,
on the authority of the rector magnificus,
prof. dr. H. Brinksma,
on account of the decision of the graduation committee,
to be publicly defended
on Wednesday, 3 November 2010 at 15:00hrs

by

Rameswor Shrestha
Born on 25 November 1976
in Nepal

This dissertation is approved by
the promotor Prof. dr. ir. Bram Nauta and
the assistant promotor Dr. ir. Ronan van der Zee

To my parents,

and my aunts

Contents

Chapter 1

Introduction

1.1 Brief History of Radio

The era of wireless communication began when Heinrich Hertz proved the Maxwell's theory of electromagnetism that predicted the existence of electromagnetic waves. In 1887, Hertz demonstrated the transmission and reception of electromagnetic waves as predicted by Maxwell through his experiment. His radio transmitter system consisted of a high voltage induction coil, a condenser and two brass conductors separated by a tiny gap to cause a spark discharge. Once a spark was generated, a conducting path was formed between the spark-gap and the charge could rapidly oscillate back and fourth at a frequency determined by the values of the capacitor and the induction coil. The receiver was a loop made from copper wire with a small gap in the loop. When the spark-gap transmitter generated a spark, a small spark was seen to jump the gap in the receiving coil. He could detect the radio waves few meters from the transmitter in his lab.

At that time Hertz thought his work has no practical application [1], and it was Guglielmo Marconi who used radio waves for communication and commercialized a practical system. Using an improved spark-gap transmitter, coherer-receiver and other various inventions at that time, he was able to transmit radio signals for about a mile at the end of 1895. In 1897, he established world's first radio station in England. In the same year, he formed his first company "Wireless Telegraph and Signal Company" in Britain. Marconi basically assembled inventions from Nikola Tesla, Oliver Lodge, Edouard Branly, etc., and used them to improve his radio system. Entrepreneur Marconi's company was able to transmit first trans-Atlantic radio signal in 1901, although the claim is later disputed [2]. He established the first permanent transatlantic wireless services from Clifden, Ireland to Glace Bay, Nova Scotia, Canada in 1907.

The importance and usefulness of wireless communication was further highlighted following the sinking of the RMS Titanic in 1912, including communications between

operators on the sinking ship and nearby vessels, and communications to shore stations listing the survivors [3]. Distress signal using wireless telegraphy from the Titanic made a great impression on the public regarding the usefulness of wireless communications.

The invention of the triode vacuum tubes by Lee De Forest in 1907 was a great step forward toward better transmitters and receivers. One terminal of the triode, called grid, controlled the current and made amplification possible. This allowed for amplitude modulation of a continuous wave signal and made voice transmission practical. Transmission with continuous wave signal is narrowband whereas spark-gap transmitters emitted wideband signals causing a serious interference problem. With an improved triode, the transmitters were made more power efficient. In 1921, the Detroit police experimented with one way voice transmission to cars. Two-way police radio, with the equipment occupying most of the car trunk, began in mid 1930s.

World War II resulted in the mass production of radio equipment in order to equip the increasing number of aircrafts and ships. The widespread use of wireless communication using telegraph, broadcasting, telephones, and point to point radio links, was accelerated during and after the war.

The invention of the transistor, drastically reducing the size and power consumption of the radio system, started a new era in electronics. By 1966, the first pocket-sized mobile phones were produced. After 1980, cellular phones and cordless phones became very popular and enjoyed very rapid growth till date.

Today, developments in radio technology are as exciting as Marconi's first transatlantic wireless communication. Recently, the International Telecommunication Union (ITU) predicted that the number of mobile cellular subscribers worldwide will reach the 5 billion mark by the end of 2010. This is an astonishing number, comparing with the world population of 6.87 billion. Another exciting example of the use of radio waves is in the space exploration. For example, NASA collects observations from the twin Voyager I and II spacecraft, which are over 12 billions kilometers away from the earth and at the edge of our solar system. It takes over 14 hours for the signal to reach the earth from the Voyager I.

1.2 Spectrum Scarcity and Usage

Early wireless telegraph communication had a moderate messaging rate of about 25 words per minute using Morse code signaling. This is equivalent to about 20bps of data rate. So the information bandwidth was just 10s of Hertz where as spark-gap transmitter emitted 100s of kHz wideband band signals. Spectral efficiency was very poor and interference was a serious problem. After the establishment of world's first spectrum regulatory body in 1934, the Federal Communications Commission (FCC) in the United States, radio transmissions needed to be licensed and separated in frequency, and were not allowed to cause interference to other users. Since its establishment, it assigns users to specific frequencies. These include AM, FM, short wave and citizen bands and VHF and UHF television channel, radio amateurs, cellular and cordless telephones, air traffic

control radars, security alarms, radio controlled toys etc. Demand for spectrum continues to grow.

The FCC frequency allocation chart [4] now shows a heavily crowded spectrum with virtually all usable radio frequency bands already licensed to commercial operators and government entities for specific services, making spectrum a scarce resource. Two different trends for the *optimal spectrum utilization* are discussed in this section.

1.2.1 Spectral efficiency enhancement trends

Spectrum bandwidth can be very expensive, at least in some mobile communication scenarios. For example, Vodafone paid $9 billion to acquire a license for UMTS operation for 2×15MHz bandwidth in the United Kingdom through auctions [5]. On the other hand, the demand for high data rates is increasing rapidly for wireless communications. So modern radio transmission and networking technologies should offer very high data rates within a limited available bandwidth, and thus increase the spectral efficiency.

A straight forward way to provide higher data rates within a given bandwidth is the use of higher-order modulation, thereby allowing more bits of information to be encoded per modulation symbol. For example in case of Quadrature Phase Shift Keying (QPSK) modulation scheme, the modulation alphabet consists of four different signaling alternatives. So QPSK allows for 2 bits of information to be communicated in each symbol. Similarly, 16QAM (Quadrature Amplitude Modulation) modulation scheme has sixteen different signaling alternatives. Thus it allows 4 bits of information to be encoded in each symbol. 64QAM modulation scheme allows 6 bits of information to be communicated in each symbol. So theoretically the spectral efficiency (bits/s/Hz) of 16QAM and 64QAM modulation is two and three times that of QPSK respectively. However the process of concentrating more and more bits per symbol cannot go on without limit. While the bandwidth utilization goes up, higher order modulation schemes such as 16QAM and 64QAM require a higher signal-to-noise ratio at the receiver for a given bit error rate (BER) compared to QPSK.

Another way to increase the data rates, without suffering from increased signal corruption is to increase the overall transmission bandwidth by means of multiple-carrier transmission. In multi-carrier transmission, many narrowband signals often called sub-carriers, which are modulated by different data stream, are frequency multiplexed and jointly transmitted over the same radio link to the same receiver. By using N-sub-carriers, the overall data rate is increased by N times. One special case of multi-carrier transmission is Orthogonal Frequency Division Multiplexing (OFDM) transmission. It utilizes the available bandwidth efficiently by employing a number of closely spaced orthogonal carrier frequencies with a total symbol rate near the Nyquist rate. Generally OFDM has a nearly ‘white spectrum’. Modern wireless communication standards increasingly use more and more complex modulation schemes and multiple carriers in order to increase spectral efficiency.

A general drawback of higher order modulation scheme and multi-carrier evolution is the large peaks in the instantaneous signal power. With the higher order modulation scheme such as 16QAM and 64QAM, the information is encoded in the instantaneous amplitude as well as phase of the modulated signal. As a result, the modulated signal will have large variations in the instantaneous power, thus the larger peaks. Probability of the larger peaks in the instantaneous power is higher for high order modulation [6] at a given average power. The ratio of the peak power to the average power of the signal which is called Peak to Average Power Ratio (PAPR) is higher for 64QAM than for QPSK modulated signal. Similarly the parallel transmission of multiple carriers will also lead to a larger variation in instantaneous transmitted power and thus to a higher peak to average power ratio. Table 1.1 shows the modulation format, PAPR, peak data rate and channel bandwidth for a number of widely used standards. The PAPR can be as high as 10dB in the case of WLAN signals.

Standards	Modulation Format	Operating Frequency	PAPR	Peak Data Rate	Channel Bandwidth
GSM (2G)	GMSK	900MHz, 1800MHz, 1900MHz	0dB	22.8kbps (9.6kbps nominal)	200kHz
GSM EDGE (2.5G)	8-PSK	900MHz,1800MHz, 1900MHz	3.2dB	59.2kbps/time slot	200kHz
WCDMA/UMTS (3G)	QPSK (downlink) OCQPSK (uplink)	1920-1980 MHz 2110-2170 MHz	3.5-7dB	2Mbps	5MHz
CDMA2000 (3G)	QPSK/BPSK/8-PSK /16QAM (adaptive)	450, 700, 800, 900, 1700, 1800, 1900, 2100 MHz	4-9dB	3.1Mbps	1.25MHz
IEEE 802.11b (WLAN)	DBPSK, DQPSK,CCK	2.4GHz (ISM)	As high as 10dB ($10\log_{10}$(N) dB, N=carriers)	11Mbps	20MHz
IEEE 802.11g (WLAN)	BPSK,QPSK, 16-QAM, 64-QAM,OFDM	2.4GHz (ISM)	As high as 10dB ($10\log_{10}$(N) dB, N=carriers)	54Mbps	20MHz
IEEE 802.11a (WLAN)	BPSK,QPSK, 16-QAM, 64-QAM,OFDM	5.1-5.8GHz	As high as 10dB ($10\log_{10}$(N) dB, N=carriers)	54Mbps	20MHz

Table 1.1: Modern standards demanding a high peak to average power ratio (PAPR)

Amplifying signals with a large peak to average power ratio using a conventional linear Power Amplifier (PA) can satisfy the linearity requirement but suffers from poor efficiency because these power amplifiers inherently operate far below their saturated output power level where the efficiency is maximum. High power efficiency is especially important for portable devices due to the desire for longer battery life. So for such applications modern power amplifiers should overcome the traditional linearity-efficiency trade-offs.

1.2.2 Spectrum sharing trends

As mentioned earlier, most of the spectrum (below 5GHz) for wireless communication is densely allocated by regulatory bodies, making bandwidth a scarce resource. As the demand for RF spectrum continues to grow, it is unlikely that the bandwidth requirement of new technologies can be met. As a result spectrum access can slow down the development of emerging radio services that can greatly improve our life style, health, safety, education of people, and work environment. However, on the other hand studies suggest that the spectrum bandwidth of most wireless communication systems is not utilized for a significant amount of time at a given location [7]. For example, the spectrum for commercial mobile communications is used heavily. But the spectrum utilization for amateur radio is poor. So, spectrum scarcity is in fact due to the inefficiency of the fixed frequency allocation pursued by our radio regulators. As an example, the situation can be compared with a busy highway where one lane is allocated for ambulance; another lane is allocated for fire-fighting vehicle and so on. The lanes for the ambulance and the fire-fighting vehicle are rarely used and most of the time free where as remaining lane is heavily used, often with traffic problems.

In order to overcome this problem, dynamic spectrum access with cognitive radio technologies, which is now one of the developments taking place, can be a revolutionary approach to increase the efficiency of spectrum usage as it redefines the traditional frequency allocation approach. It allows unlicensed wireless users (secondary users) to operate in the licensed bands from legacy spectrum holders (primary users) on a negotiated or an opportunistic basis without harmful interference or disturbance to the communications of the primary users. By actively monitoring the radio frequency environment, radio terminals dynamically select empty frequency spectrum and change transmission and reception parameters like power, frequency, modulation etc accordingly. Engineers and scientist around the world are now working to bring that kind of flexible, adaptive and reconfigurable system with operating intelligence to future radios. The idea of cognitive radio was described by Joseph Mitola in [8]. As current demand for spectrum looking to increase, some regulatory bodies like FCC in the USA and Ofcom in the United Kingdom are looking favorably at the idea of cognitive radio. It has the potential to alleviate the spectrum scarcity.

In addition to the high level of processing required for the cognitive radio realization, a hardware platform is needed to be particularly flexible, allowing for flexible choice of the radio frequency depending on free available spectrum. Traditional hardware can not handle this requirement because they are band limited, optimized primarily for low cost and low power, and not flexible.

1.3 Software-Defined Radio Transmitters

In recent years, the explosive growth in the wireless market has led to wireless transceiver terminals that have multiple applications and cover multiple standards. Nowadays, it is not uncommon to have tri- or quad-band GSM, WCDMA, IEEE 802.11a/b/g wireless LAN, Bluetooth, and GPS in the same phone. Much more

functionalities are expected to be added in the future. The current approach of multi-standard radio is to use multiple transceivers with their own RF and baseband circuitry, one for each standard.

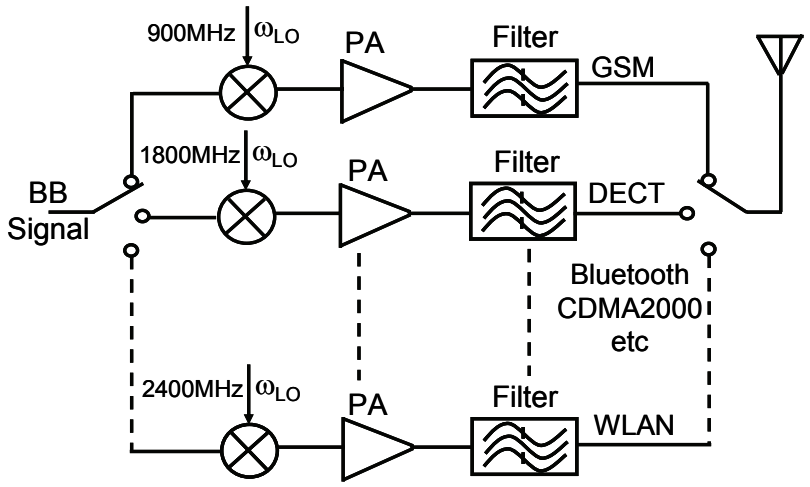


Figure 1.1: Conventional multi-standard transmitter architecture

Fig. 1.1 shows a typical example of a multi-standard transmitter, with multiple narrow-band power amplifiers which are limited in bandwidth mainly by *dedicated filters*, one for each standard, selectable by a switch. With the ever increasing number of different standards to be supported, this architecture becomes increasingly unpractical, as support for every new frequency band requires adding external dedicated components and more die area. A dream is to have a much more flexible radio, which can support many different standards. If you insist on a visionary view: we aim for "the holy grail of software radio". A software defined radio is the radio in which some or all of the physical layer functions are software-defined [9]. Cognitive radio can also be viewed as an extension of a software-defined radio. So as in the case of cognitive radio, a software-defined radio needs a flexible or reconfigurable hardware platform to allow for a flexible choice of the radio frequency. One of the main obstacles in implementing a flexible or reconfigurable transmitter is the fixed frequency output filter, needed to suppress the strong harmonics generated by the power amplifier to acceptable levels.

1.4 Scope of this thesis

In section 1.2 and 1.3, we discussed two separate problems in modern wireless communication systems that are mainly related to the power amplifiers for the radio front-end; (a) a transmitter power efficiency problem amplifying signals with a large PAPR and (b) a lack of flexible RF front-ends to choose an arbitrary RF transmitter frequency. In this thesis, we separately cover solutions to these two different problems. The scope is limited to the RF front-end of the transmitter.

1.5 Outline

In chapter 2, the properties of a complex digital modulated signal and different methods to measure the linearity and efficiency of power amplifiers is discussed. This chapter also presents the basic power amplifiers classes and efficiency enhancement techniques. Similarly, different ways to obtain a flexible RF transmitter front-end with the focus on the power amplifier and RF output filter are explained.

In chapter 3, a detailed analysis of the polyphase multipath circuit technique is presented. The technique is applied to realize a wideband *filter-less* power upconverter by canceling a very large multitude of harmonics and sidebands. The design is realized in a 0.13µm CMOS process which mainly focuses on a proof-of-concept of the polyphase multipath technique. This chapter also presents measurement results of the demonstrator chip.

In chapter 4, the design of a polar modulated power amplifier, which is one of the efficiency enhancement techniques, is presented. First, the main challenges in implementing a polar modulated PA are explained. Then, the overview of the system to overcome those challenges is given. This chapter also discusses the design of the supply modulator, one of the tough building blocks in a polar modulated PA. Finally, the measurement results of the prototype chip fabricated in a 65nm CMOS with the off-chip passive components on a laminate module is presented in this chapter.

Chapter 5 offers conclusions and presents suggestions for future work.

References

[1] G.R.M. Garratt, "*The early history of radio: from Faraday to Marconi*", London, Institution of Electrical Engineers in association with the Science Museum, History of technology series, 1994

[2] J.S. Belrose, "Fessenden and Marconi: Their Differing Technologies and Transatlantic Experiments during the First Decade of this Century", *International Conference on 100 Years of Radio*, 5-7 September 1995

[3] T. H. White, "United States Early Radio History" (online): http://earlyradiohistory.us

[4] NTIA, "FCC Frequency Allocation Chart", 2003; (online): http://www.ntia.doc.gov/osmhome/ allochrt.pdf

[5] K. Binmore and P. Klemperer "The Biggest Auction Ever: the Sale of the British 3G Telecom Licences", *Economic Journal*, pp 74-95, March 2002

[6] E. Dahlman, S. Parkvall, J. Sk¨old, and P. Beming, "3G Evolution: HSPA and LTE for Mobile Broadband", Academic Press, Oxford, UK, 2007

[7] FCC Spectrum Policy Task Force, “Report of the spectrum efficiency working group”, (Online): http://www.fcc.gov/sptf/reports.html, Nov. 2002

[8] J. Mitola, “Cognitive Radio: An Integrated Agent Architecture for Software Defined Radio” Ph.D. dissertation, KTH, Stockholm, Sweden, December 2000

[9] SDR Forum, “SDRF Cognitive Radio Definitions”, (online): http://www.sdrforum.org/pages/documentLibrary/documents/SDRF-06-R-0011-V1_0_0.pdf

Chapter 2

Linearity, Efficiency and Flexibility of RF Power Amplifiers

The Power Amplifier is often one of the most power consuming building blocks in a portable device. It is also the last building block that determines the quality of the transmitted signal. So, on one hand a power amplifier has to be efficient to increase the talk time or the battery life time and on the other hand the transmitted signal should satisfy the linearity requirements.

The type of modulation used in a particular standard has a great impact on the design of a power amplifier. First generation analog cellular systems like the Advanced Mobile Phone System (AMPS), the European Total Access Communication system (ETACS), and the Japanese Access Communication system (TACS) use a frequency modulation scheme, which results in a constant amplitude signal [1], [2]. Similarly the Global System for Mobile Communication (GSM), the most widely accepted second generation digital cellular standard, uses a Gaussian Minimum-shift Keying (GMSK) digital modulation scheme. GMSK is a special type of phase modulation and also results in a constant amplitude signal. Since those standards use a modulation scheme that results in a constant amplitude signal, a non-linear amplifier which has a high efficiency can be used to amplify those signals. As a result, traditional power amplifier design often ignores the characteristics of the signal. Designers rather focus on optimizing the efficiency at the saturated output power by playing with the device technology and the circuit design. However, as the demand for high data rate increases rapidly, modern wireless standards are forced to use spectrally efficient complex modulation schemes and multiple carriers that contain information both in amplitude and phase. Such signals have a variable envelope with high peak-to-average power ratio. To design a power amplifier for such systems, the understanding of the characteristics of the modulated signal is necessary to optimize the power amplifiers performance in terms of both linearity and efficiency. Section 2.1 discusses different digital modulation scheme and the signal characteristic

from the power amplifier prospective. Different ways to measure the linearity of power amplifiers used to amplify complex digital signal is presented in section 2.2. In section 2.3, basic (classic) linear and switch mode RF power amplifiers are discussed. These amplifiers always have a trade-off between linearity and efficiency. Efficiency enhancement techniques that defy the traditional linearity/efficiency trade-off are explained in section 2.4. Section 2.5, finally, deals with the output filtering challenges for software defined radio and cognitive radio.

2.1 Digitally Modulated Signal Characteristic

In digital modulation, a digital data stream is modulated with an analog carrier signal. Figure 2.1 shows a typical transmitter architecture used in a digital wireless communication system. A digital baseband processor generates an in-phase (I) and a quadrature phase (Q) component from the stream of bits that need to be transmitted. The baseband signal is then frequency up-converted to RF by using a quadrature modulator. In the quadrature modulator, I and Q signals are modulated with the in-phase and the quadrature-phase carriers respectively. The outputs are then summed up to yield the modulated signal:

$$S(t) = I\cos(2\pi f_c t) - Q\sin(2\pi f_c t) \quad \textbf{(2.1)}$$

where f_c is the carrier frequency.

The modulated bandpass RF signal of equation (2.1) can also be represented in polar form by:

$$S(t) = A(t)\cos(2\pi f_c t + \varphi(t)) \quad \textbf{(2.2)}$$

Where $A(t) = \sqrt{I^2 + Q^2}$ and $\varphi(t) = \tan^{-1}\left(\frac{Q}{I}\right)$

The modulated RF signal is then amplified by a power amplifier before it is fed to antenna.

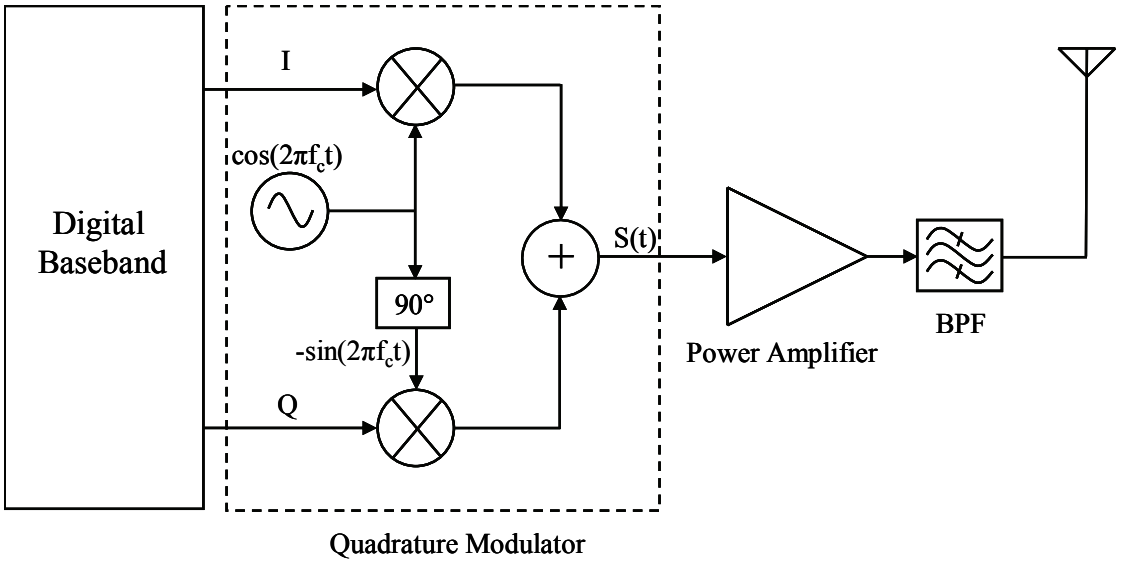


Figure 2.1: Typical linear transmitter architecture

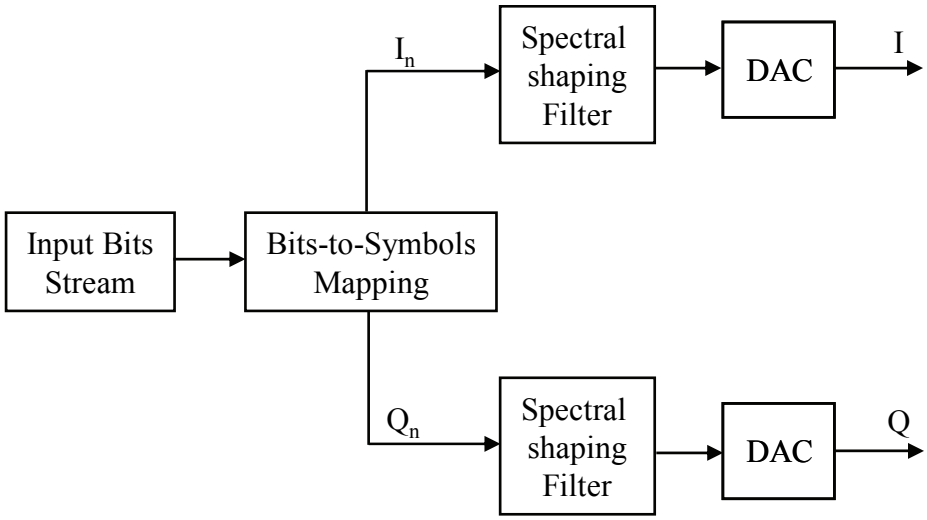


Figure 2.2: A typical block diagram of a digital baseband

In a digital baseband circuitry as shown in Figure 2.2, incoming bits stream are mapped into unique symbols that contains an in-phase (I_n) and a quadrature-phase (Q_n) component. Symbols are vectors. It can be represented in an IQ-plane. The placement of symbol constellation points in the IQ-plane is based on the modulation format, a pattern used to map the incoming bits. Figure 2.3 shows constellations pattern in the IQ-plane for various modulation formats. One or more bits can be encoded in each symbol, depending on the modulation format. Some common types of digital modulation format are:

i) Phase Shift keying (PSK): In PSK modulation, the phase of a carrier signal is varied to represent the information to be sent. As a result, constellation points in the IQ plane are distributed on the unit circle. One of the simplest forms of this kind of modulation is a

binary phase shift keying (BPSK) where the phase of a carrier signal changes between 0° and 180°. In an IQ diagram of BPSK, the I state has two different values to represent a binary '1' and '0' as shown in Figure 2.3(a). One of the most commonly used phase modulation scheme such as in CDMA2000 and Digital Video Broadcasting-Satellite (DVB-S) standards is a Quadrature Phase Shift Keying (QPSK). QPSK has four states: two I values and two Q values as shown in Figure 2.3(c), thus giving 2 bits per symbol. Similarly 8-PSK modulation has 8 states and modulates 3 bits per symbol.

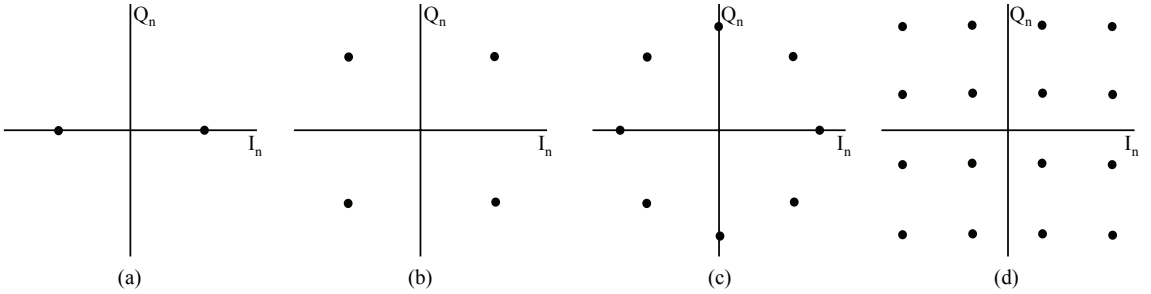


Figure 2.3: Constellation pattern in the IQ plane for a) BPSK, b) QPSK, c) 8-PSK and π/4-shifted-QPSK, d) 16QAM

Filtering: A signal with step change in phase or amplitude requires a large bandwidth. So filtering is required to transmit the digital information in the smallest possible bandwidth without introducing inter-symbol interference (ISI). The shape and bandwidth of the I and Q signal, and hence the actual signal trajectories, depend on the characteristics of the filter. Some common types of pulse shaping filters [3] are:

- Root Raised Cosine
- Half-Sinusoid
- Gaussian

Signal Trajectory: The trajectory of the transition between the states in the symbol defines some important characteristics of the modulated signal S(t). Figure 2.4(a) shows the signal transitions for QPSK modulation before filtering. From the power amplifier prospective, two things are clear from this figure. The first one is that some of the transition of states, sketched as straight line, travel through zero (origin), thus causing the amplitude of the modulated signal to also cross zero. A zero crossing can create problem in power amplifier design as it needs infinite dynamic range. The second is that the modulated signal has varying envelope as it moves to different states. So a linear amplifier is required to amplify such signal.

A special type of QPSK modulation called π/4-shifted-QPSK is proposed to avoid zero crossing of the modulated carrier signal amplitude. The signal constellation of π/4-shifted-QPSK can be viewed as a superposition of two QPSK constellations offset by π/4 relative to each other as shown in Figure 2.4(b). Symbol phases are changed from one of the QPSK constellations to the other alternatively, meaning that a QPSK constellation is shifted by π/4 radians in every alternate symbol. So a relative phase transition between states in successive symbols is either ±π/4 radian or ±3π/4 radian. This avoids the

transitions in the signal constellation to pass through origin. As a result the envelope of π/4-shifted-QPSK exhibits less variation than that of QPSK, making the signal more power amplifier friendly. There is also a differential version of π/4-shifed-QPSK called π/4-shifted-DQPSK (differential quadrature phase-shift keying) modulation in which the information is encoded in the magnitude and direction of the phase shift, not in the absolute position of the constellations. The π/4-shifted-DQPSK modulation format is used in NADC-IS-54 (North American Digital Cellular), PHS (Personal Handyphone System), TETRA (Trans European Trunked Radio), PDC (Personal Digital Cellular) and others.

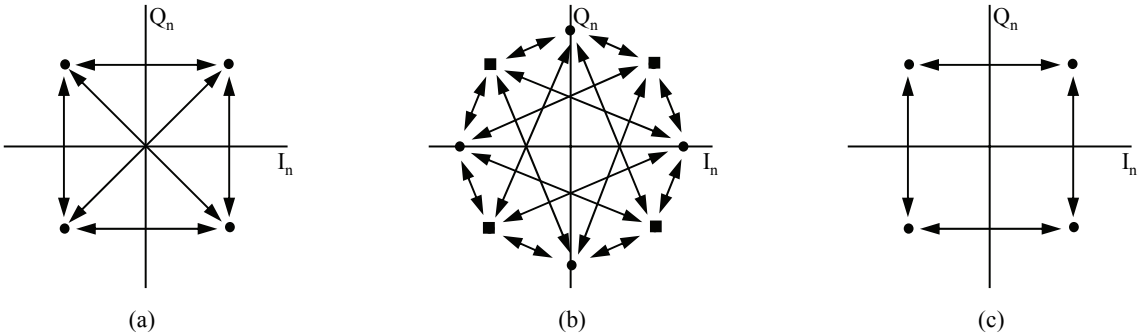


Figure 2.4: Signal transitions for a) QPSK, b) π/4-shifted-QPSK, c) OQPSK

Another important variant of QPSK is offset QPSK (OQPSK). In OQPSK, the Q signal is delayed by half a symbol period as shown in Figure 2.5(b) so that the transition of I and Q channels of the OQPSK do not occur at the same time. In the constellation diagram, signal transitions only occur to neighbors (see Figure 2.4(c)). To go through the phase transition of π, the OQPSK makes two transitions of π/2 in each half of the symbol period. Hence the maximum phase transition is π/2, and occurs twice as often, but with half the intensity of the QPSK. Square root-raised cosine pulse shaping is used in OQPSK.

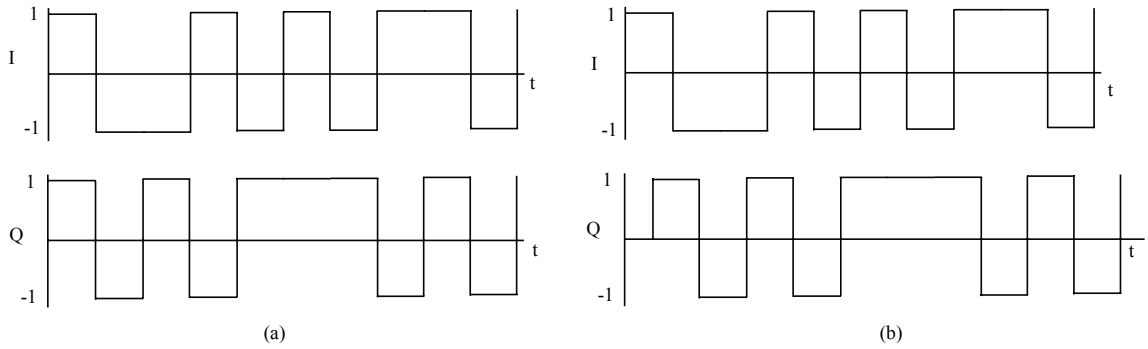


Figure 2.5 I and Q channel mappings of (a) QPSK and (b) OQPSK signal

ii) Minimum Shift Keying (MSK): MSK is related to OQPSK modulation. The difference is that MSK uses half-sinusoid pulse shaping where as OQPSK uses square root-raised cosine pulse shaping. Figure 2.6 shows MSK pulses. The MSK modulation makes the phase change continuous, with no discrete jump in phase at the symbol edge,

and limited to ±π/2 over a bit period 'T' (half symbol period). As a result the MSK modulated carrier signal has constant envelope and its power spectral density has low side lobes.

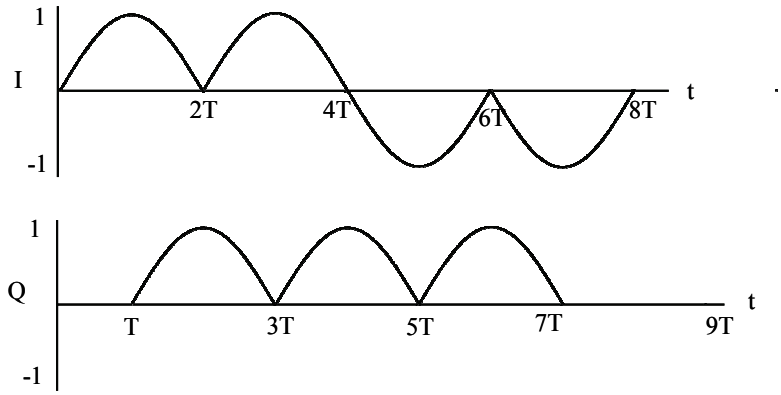


Figure 2.6 I and Q component of MSK signal

The phase transition can be made even smother by using a Gaussian pulse shaping filter. This type of modulation is called GMSK (Gaussian Minimum Shift Keying). GMSK modulated carrier signal also has constant amplitude. Highly efficient non-linear amplifier can be used to amplify such constant envelope signal. GMSK is used in GSM.

Note that although MSK and GMSK are conceptually related to OQPSK modulation, they are often classified as FSK (Frequency Shift Keying) modulation owing to the dual nature of phase and frequency modulation [3].

iii) Quadrature Amplitude Modulation (QAM): In quadarature amplitude modulation, the constellation points, typically, lie on a square lattice. As shown in Figure 2.3(d), 16QAM has four I values and four Q values resulting in 16 possible states. The modulation order of QAM can be extended to other variant like 32QAM, 64QAM, and 256QAM, representing each symbol by 5, 6 and 8 bits respectively. The transition can take place from any state to any other state at every symbol time.

Quadrature amplitude modulation is a popular family of digital modulation schemes as it can achieve high spectral efficiency. It is used in applications including Wireless LAN (WLAN), DVB-C (Digital Video Broadcasting-Cable), and Modems. However, as discussed in section I.II, as the modulation order increases, the constellation points are placed closer together and are thus subject to noise and distortion. Highly linear power amplifiers are required to amplify those signals. Unfortunately, as the modulation order increases, the peak-to-average power ratio also increases. This reduces the efficiency of a power amplifier.

2.2 Measuring Linearity and Efficiency of Power Amplifiers

The previous section described the characteristic of the digitally modulated signal with respect to the modulation format. The use of spectrally efficiency modulation schemes results in a variable envelope signal. What is important to the power amplifier designer is that the power amplifier used to amplify such signal should be sufficiently linear and efficient. This section discusses several ways to quantify linearity and efficiency of the power amplifier.

2.2.1 Measuring linearity

A power amplifier is essentially a non-linear device as it has to handle a large input/output signal with reasonable power efficiency. Non-linearity in the RF power amplifier creates two main problems: inter-modulation distortion and generation of harmonics. Inter-modulation distortion at the output results in increase bit error-rate or deterioration in EVM and interference to the nearby channels or even violation of the spectral mask. Harmonic distortion, however, in many cases can easily be removed by filtering. The consequence of a filter is that the resulting system is narrowband. Some of the widely used methods to measure the effect of non-linearities on modulated signal are follows:

2.2.1.1 Spectral Mask

The spectrum of a transmitted signal should ideally be confined to the assigned frequency band. However, the non-linearity in the transmitter causes the output spectrum to spread in the nearby channels due to the generation of inter-modulation products. Spectral masks are used by standards or regulatory bodies to define the maximum amount of interference that is acceptable. In the assigned band the spectral mask generally has a flat top representing the power level of the transmitted signal and outside the band the mask shows the limits that the transmitter should not exceed. For example Figure 2.7 shows the spectral mask requirement for the IEEE 802.11a/g WLAN standard [4].

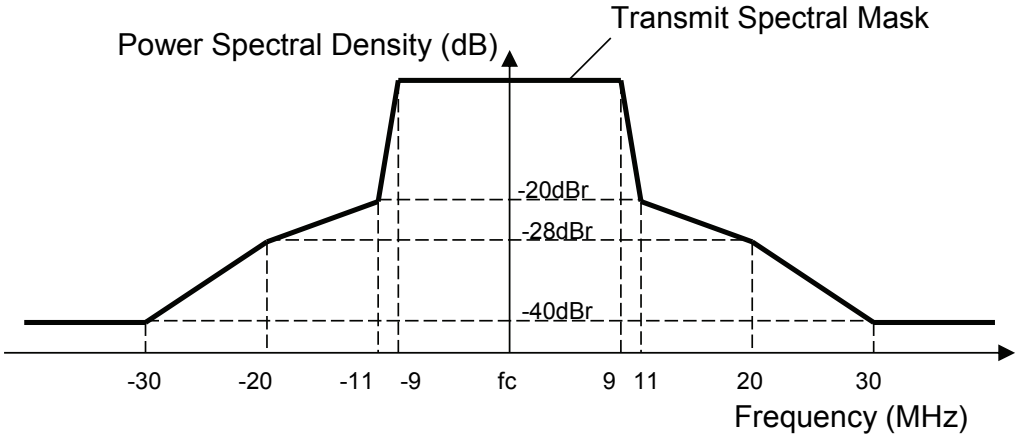


Figure 2.7: Spectral mask for the IEEE 802.11a/g WLAN standard

2.2.1.2 Error Vector Magnitude (EVM)

The error Vector Magnitude is the one of the most useful means to quantify the quality of the transmitted or received RF signals, such as digitally modulated signals. Due to various imperfections in the transmitter or receiver chain like non-linearity of the power amplifier, IQ imbalance, gain variations, noise, the constellation points of the transmitted/received signal deviate from their ideal locations. The error vector is a vector in the IQ plane between the ideal constellation point and the point that is measured or received by the receiver. EVM is the magnitude of the error vector, normalized to the signal voltage. As shown in Figure 2.8, EVM is given by,

$$EVM = \left| \frac{\vec{e}}{\vec{r}} \right| \tag{2.3}$$

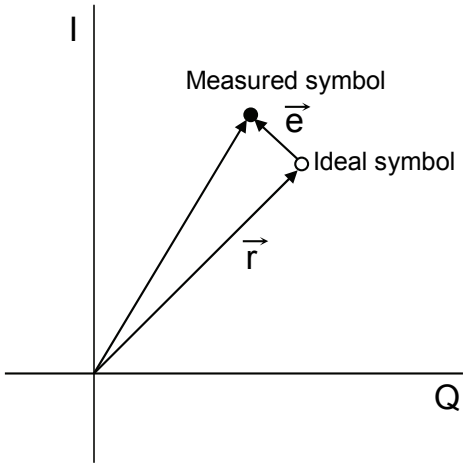


Figure 2.8: Error Vector representation

For non-constant amplitude modulation schemes such as QPSK, QAM etc, rms EVM is the root-mean-square power of all error vectors normalized to the reference power. The reference power is the power of the outermost (highest power) symbol, or the average constellation power, or the average reference signal power depending on the particular standard. For IEEE 802.11a/g standard the rms EVM is averaged over subcarriers, OFDM frames and packets, and normalized to the average power of the constellation [4]. The following equation is used to calculate the EVM:

$$Error_{rms} = \frac{\sum_{i=1}^{N_f} \sqrt{\frac{\sum_{j=1}^{L_p} \left[\sum_{k=1}^{52} \left\{ (I(i,j,k) - I_o(i,j,k))^2 + (Q(i,j,k) - Q_o(i,j,k))^2 \right\} \right]}{52 L_p \times P_0}}}{N_f} \tag{2.4}$$

where
L_p is the length of the packet;

N_f is the number of frames
$I(i,j,k)$, $Q(i,j,k)$ denotes the received symbol points of the i^{th} frame, j^{th} symbol, k^{th} subcarrier of the OFDM symbol in the complex plane
$I_0(i,j,k)$, $Q0(i,j,k)$ denotes the ideal constellation points of the i^{th} frame, j^{th} symbol, k^{th} subcarrier of the OFDM symbol in the complex plane
P_0 is the average power of the constellation
Number of subcarriers are 52 (48 data +4 pilot)

The resulting relative constellation RMS error should be smaller than -25dB for 54Mbps data rate (64QAM).

2.2.1.3 Adjacent Channel Power Ratio (ACPR) or Adjacent Channel leakage Ratio (ACLR)

Adjacent Channel power Ratio is also a widely used metric to indicate the interference to the adjacent channel caused by the non-linearity of power amplifier.

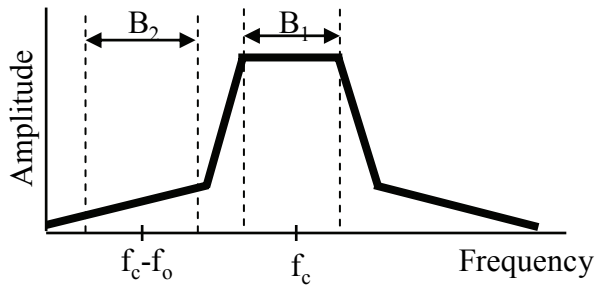


Figure 2.9: ACPR measurement

ACPR is the ratio of the power contained in a defined bandwidth (B_2) of the adjacent channel at a defined offset (f_o) from the channel centre frequency (f_c) to the power in the defined bandwidth (B_1) of the main signal [5] as shown in Figure 2.9. The bandwidths B_1 and B_2 are not necessarily the same. The ACPR test quantifies the energy of a digitally modulated RF signal that spills from the intended communication channel to the adjacent channel. For many of the current and future transmission standards including CDMA, WCDMA, NADC uses ACPR to characterize distortion generated by the nonlinearity of transmitter circuits. Since power amplifier is the most nonlinear block in the transmitter chain, many power amplifier test systems require measuring this quantity.

2.2.1.4 Noise Power Ratio (NPR)

Noise power ratio is the measure of in-channel distortion power caused by the non-linearity of amplifiers. The NPR measurement is an effective way of testing the linearity performance of amplifiers operating with many carriers (>10). For the NPR measurement, white noise is first passed through a bandpass filter to produce an approximately square pedestal of noise. The width of the noise pedestal is usually made equal to the bandwidth of the channel under test. Then this signal is passed through a notch filter to get the noise

pedestal with a deep notch, typically >50dB, as shown in Figure 2.10. This noise signal is used to excite the test PA.

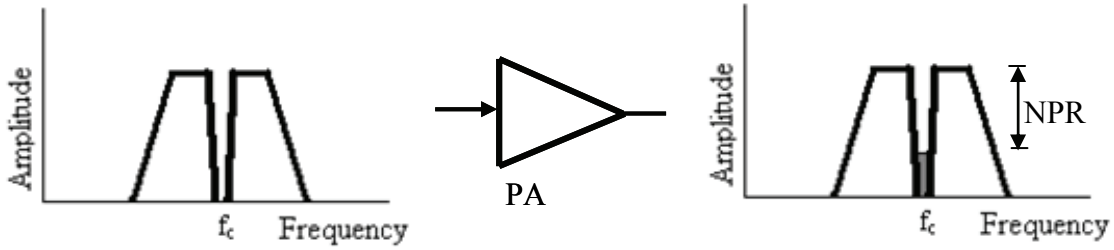


Figure 2.10: Noise power ratio measurement

At the output, the noise pedestal in the notch tends to fill due to the non-linearity of the PA. The depth of the notch at the output of the PA as shown in the Figure 2.10 is a measure of the NPR.

2.2.2 Efficiency measurement

The efficiency of an amplifier is a measure of how effectively DC power is converted to RF power. The efficiency is a critical factor in power amplifier design, especially in a battery operated mobile devices. Different terms are used to describe the efficiency. Some of the most common definitions are presented below:

2.2.2.1 Drain Efficiency

Drain efficiency is defined as the ratio of RF output power to dc input power.

$$\eta = \frac{P_o}{P_{dc}} \tag{2.5}$$

It does not take into account the RF input power. So, in the case of a RF amplifier with low gain this is not a convincing measure for efficiency.

2.2.2.2 Power Added efficiency (PAE)

The definition of power added efficiency includes the effect of the drive power and gives a reasonable indication of power amplifier performance even when the gain is not high. The PAE is defined as

$$PAE = \frac{P_o - P_{IN}}{P_{dc}} = \frac{P_o - \frac{P_o}{G_p}}{P_{dc}} \tag{2.6}$$

where $G_p = \frac{P_o}{P_{IN}}$ is the power gain

The PAE is most useful for constant amplitude signals.

2.2.2.3 Overall efficiency

Overall efficiency is an alternative definition of PAE which also includes the effect of drive power.

$$\eta_{OVERALL} = \frac{p_o}{p_{dc} + P_{IN}} = \frac{P_o}{P_{dc} + \frac{P_o}{G_p}} \tag{2.7}$$

Overall efficiency is always positive, whereas PAE can be negative if the amplifier gain is less than 1.

2.2.2.4 Average efficiency

The above three definitions of efficiency are for a sinusoidal input and output (constant-envelope) signal. For most power amplifiers, the efficiency is highest at the peak output power and decreases as output/input decreases. However, most of the time power amplifiers operate far below the peak output power when amplifying a digitally modulated signal with high peak to average ratio as illustrated in Figure 2.11. When the envelope of the input signal is time-varying (non-constant), the efficiency is also a time-varying. So, a good method to measure the performance of the power amplifier is the average efficiency. It is the ratio of the average output power to the average dc input power.

$$\overline{\eta_{AVG}} = \frac{\overline{P_o}}{\overline{P_{dc}}} \tag{2.8}$$

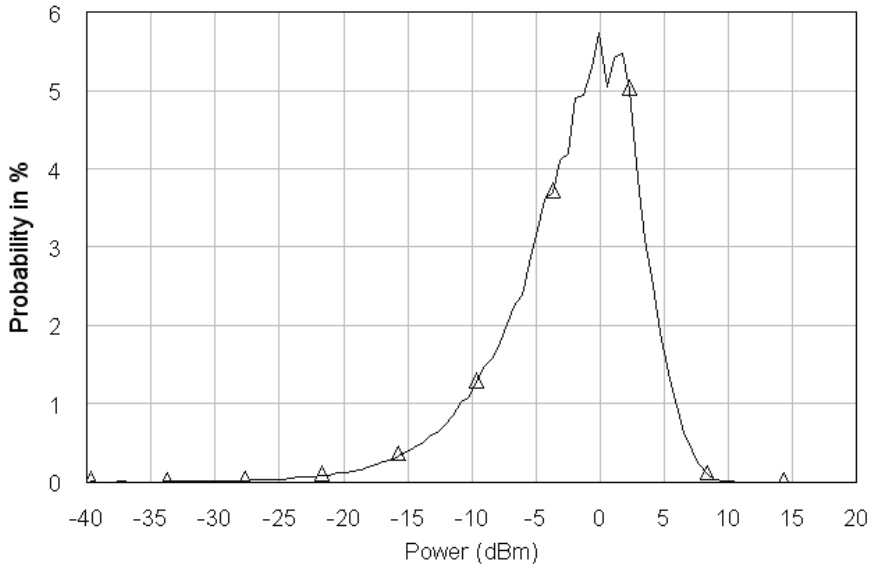


Figure 2.11 Probability distribution of output power occurrence in IEEE 802.11a/g signal

The average input and output power can be calculated as [6]

$$\overline{P_i} = \int_0^{P_{out,\max}} P_{dc}(P_{out}) PDF(P_{out}) dP_{out} \quad \textbf{(2.9)}$$

and

$$\overline{P_o} = \int_0^{P_{out,\max}} P_{out} PDF(P_{out}) dP_{out} \quad \textbf{(2.10)}$$

Where $PDF(P_{out})$ is the probability that the amplifier will have an output power P_{out} and $P_{dc}(P_{out})$ is the dc input power required at P_{out}.

Average efficiency is very useful in a case that is precisely formulated. It is the measure of how effectively the PA converts the stored energy in the battery into transmitted energy. So, it is directly related to the battery life in mobile handsets. However, it does not take peak current or power into account.

2.3 Basic Linear and Switch Mode Power Amplifiers

The previous section described several ways to quantify linearity and efficiency performance of power amplifiers. There is a fundamental tradeoff between linearity and efficiency in a standalone power amplifier, depending on its class. This section briefly discusses different classes of power amplifiers.

Power amplifiers are generally classified based on the circuit configuration and the conduction angle into different classes such as A, AB, B, C, D, E, F and so on. Normally these classes of PAs can be placed in two categories: Linear Mode and Switch Mode PAs. In linear mode PAs, the device normally acts as a transconductor. The relationship between input and output, however, may not be linear. In switch mode PAs, the device acts as a switch.

2.3.1 Linear mode Power Amplifiers

The amplifier classes in this mode are differentiated based on the conduction angle, which is defined as the period at which the power device is conducting. Class-A, -B, -AB and -C belong to this category. Figure 2.12 shows the basic circuit topology for a linear mode power amplifier. By varying bias voltages and input drive power, the conduction angle can be chosen between 0 and 360°. The corresponding classes are defined as:

- Class-A amplifiers, if the conduction angle =360^o.
- Class-B Power Amplifiers, if the conduction angle=180^o.
- Class-AB Power Amplifiers, if 180^o< conduction angle< 360^o.
- Class-C power Amplifiers, if the conduction angle <180^o.

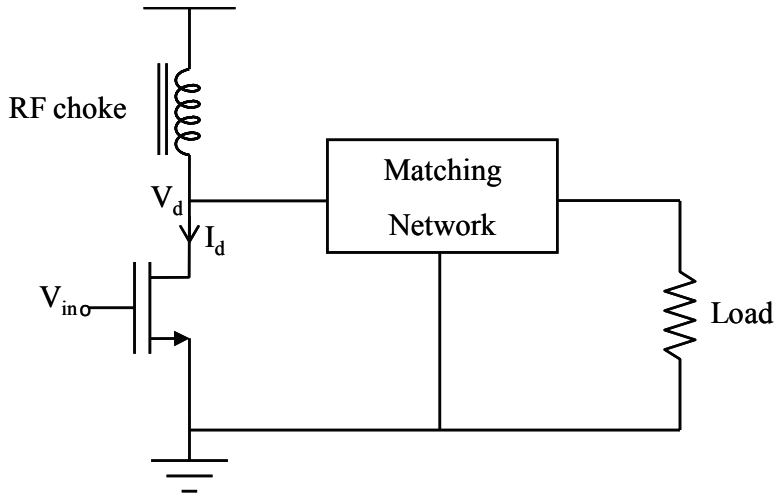


Figure 2.12: Basic Circuit of single-ended class-A, B, AB, or C amplifier

Class-A Power Amplifiers

In a class-A power amplifier, the power device is biased such that the transistor remains in the transconductance region during the entire RF cycle, which means the conduction angle is 360^{o}. As a result, class-A power amplifiers have the highest linearity and power gain compared to other amplifier classes. However, due to the bias point in the middle of the transconductance region of the I-V curves, a large quiescent current flows into the device resulting in huge power dissipation. The theoretical maximum power efficiency is 50%. Drain current and voltage waveforms of an ideal class-A amplifier [7], [8] are shown in Figure 2.13.

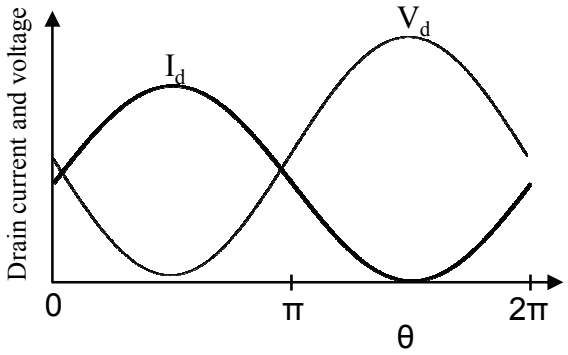


Figure 2.13: Ideal drain current and voltage waveforms of a class-A power amplifier

In summary, Class-A PAs have high linearity, high gain, wideband operation, high frequency operation and poor efficiency.

Class-B Power Amplifiers

In class-B operation the gate of the power transistor is biased at the threshold voltage (zero quiescent current) so that the drain current flows during only one half of the input

sinusoidal signal, resulting in a conduction angle of 180 °. Figure 2.14 shows the drain current and voltage waveforms of an ideal clas- B amplifier.

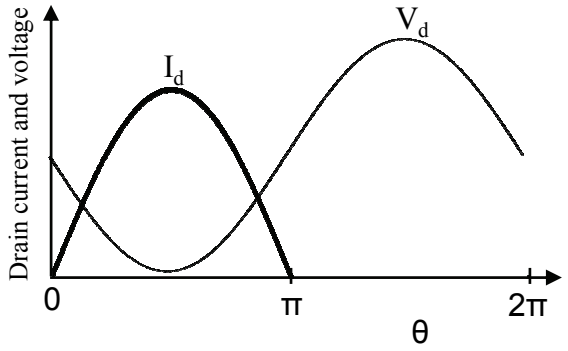


Figure 2.14: Ideal drain current and voltage waveforms of a class-B power amplifier

Mostly, class-B amplifiers are designed in push-pull configuration so that each transistor conducts for each half cycle and the two drain currents add together to produce a sine-wave output. But linearity, output harmonic content, and intermodulation distortion are not as good as in class-A. However, the maximum efficiency of a class-B amplifier is considerably higher, theoretically 78.5%. In practice, to reduce the crossover distortion, the transistor is biased at a small quiescent current, typically 1-10% of the peak drain current. Thus, practical devices in principle operate in class-AB.

Class-AB Power Amplifiers

A class-AB power amplifier is a good compromise between a class-A and a class-B amplifier and is biased such that the conduction angle is between 180 ° and 360 °. The linearity of class-AB amplifiers is close to that of class-A amplifiers while the efficiency is close to that of class-B amplifiers. The bias point for those amplifiers is selected depending on the linearity and efficiency requirements.

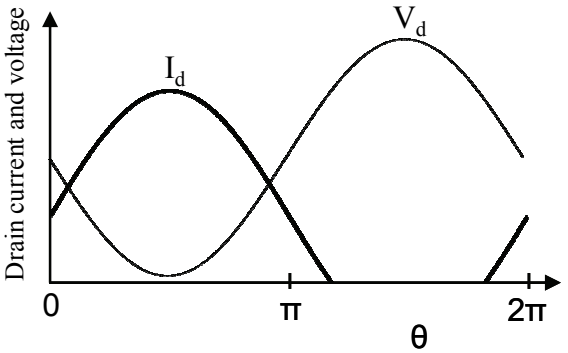


Figure 2.15: Ideal drain current and voltage waveforms of a class-AB power amplifier

Class-C Power Amplifiers

The gate of the power transistor in a class-C power amplifier is biased below the threshold so that the transistor is active for less than half of the RF cycle. The efficiency is higher than that of class-A, B, and AB. The theoretical maximum efficiency reaches towards 100% by decreasing the conduction angle toward zero. But at the same time, output power decreases towards zero. This class of PAs is highly non-linear in high efficiency operation. One main advantage of class-C amplifier in comparison to switch mode PA is that the output amplitude varies with the input amplitude. This means the class-C amplifier can be used to amplify variable envelop signals, keeping the possibility to get high efficiency without varying the supply voltage [9]. For switch mode PAs, the only way to control the output power is by varying the supply voltage.

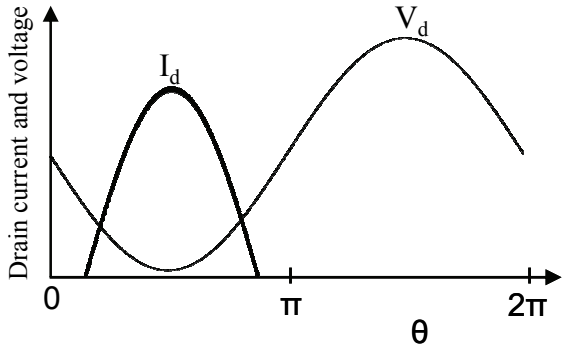


Figure 2.16: Ideal drain current and voltage waveforms of a class-C power amplifier

2.3.2 Switched Mode Power Amplifiers

In switch mode power amplifiers the device acts as a switch. Those power amplifiers are highly non-linear and known for high efficiency. The theoretical maximum efficiency is 100%.

Class-D Power Amplifiers

Figure 2.17(a) shows a typical class-D amplifier circuit. Class-D amplifiers use two active devices which act as a two pole switch that connect the load network to ground and supply alternately. With this push-pull operation, a rectangular voltage waveform is generated at the drain. The LC tank circuit passes only the fundamental components to the load. Figure 2.17(b) shows the drain current and voltage waveform in an ideal class-D operation.

The ideal maximum efficiency of class-D PA is 100%. However in practice it suffers losses from ON-resistance, finite switching time and drain capacitance. Class-D amplifiers are used extensively in audio applications, but are seldom used above VHF due to the high switching loss.

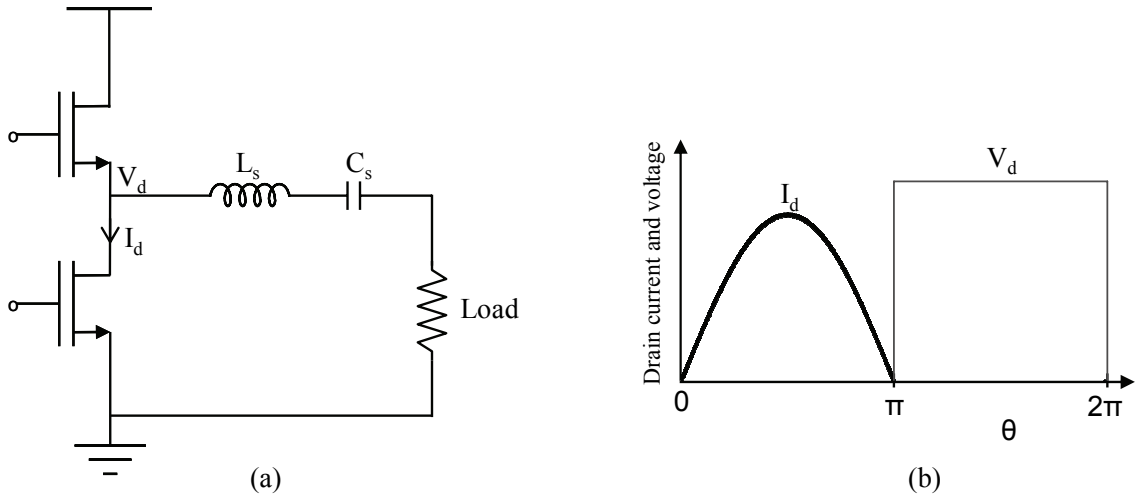


Figure 2.17: a) Class-D amplifier and b) its waveforms at the output node

Class-E Power Amplifiers

The basic schematic of a class-E amplifier is shown in Figure 2.18(a). It uses the idea of soft switching and usually employs a single transistor as a switch. The class-E PA tries to force the voltage across the output node (V_d) to zero with zero slope at the instant when the switch is closed (as shown in Figure 2.18(b)) so that there is no switching loss [10]. The most common matching network consists of a series tuned LC circuit and shunt capacitor across the switch. One of the big advantages of this amplifier is that the drain-source capacitance of the transistor can be used as the one of the circuit component in the matching network. So the transistor's drain-source capacitance is no longer a source of power loss as in the case of class-D but becomes an important part of the circuit operation. For this reason, the class-E amplifier is used in very high frequency applications.

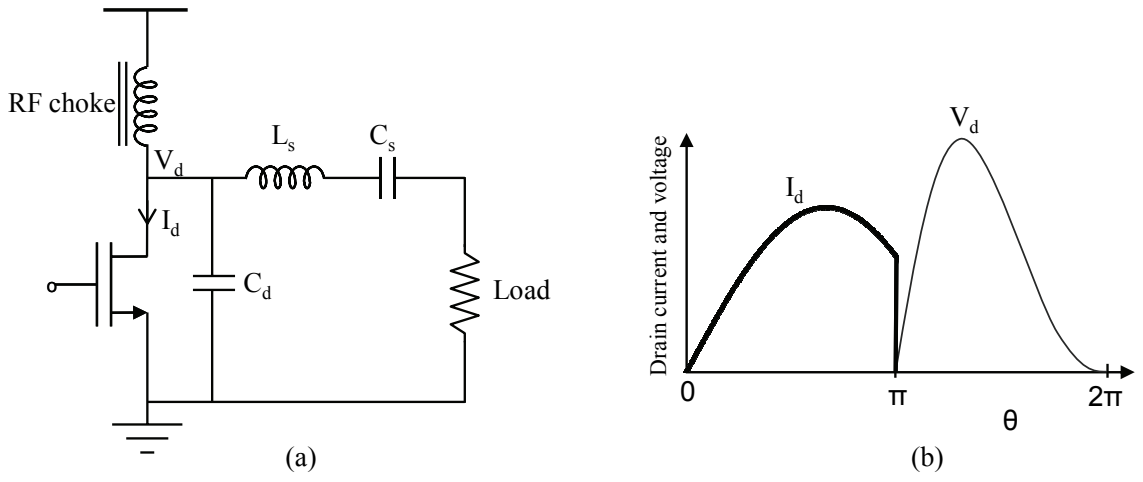


Figure 2.18: a) Class-E power Amplifier and b) its waveform at the output node

Class-F Power Amplifiers

The class-F PA is distinguished by the matching network which consists of multiple harmonic resonant filters. For ideal operation of Class-F amplifiers as shown in Figure 2.19(a), the matching network should be such that it blocks all the odd harmonics, and shorts all the even harmonics. The addition of harmonic components shapes the drain waveforms to square at the output of the active device as shown in Figure 2.19(b), thus eliminating loss in the switch. This makes class-F amplifiers suitable for high frequency operation. However in practical applications, the harmonic tuning is applied only up to the third or fifth harmonic, to reduce the matching network circuitry. Consequence of this is a little degradation in efficiency due to some overlap between the drain current and voltage.

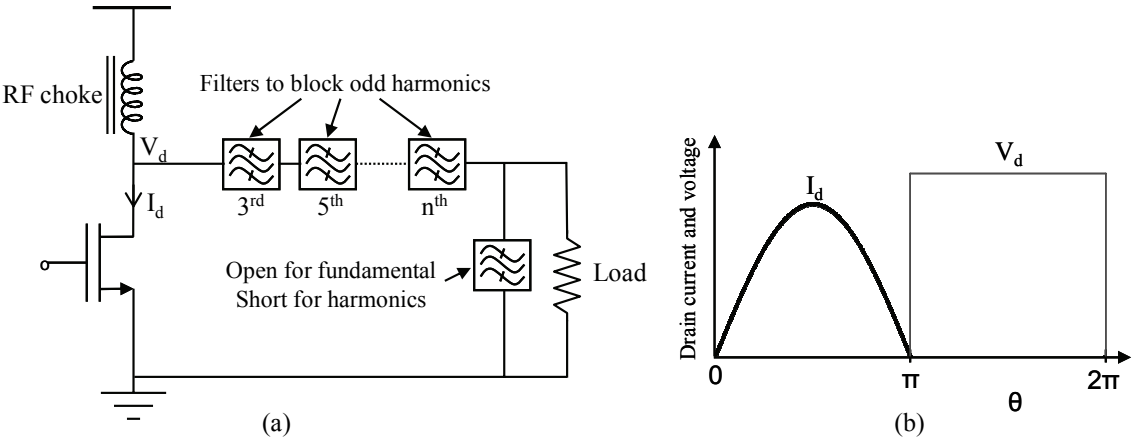


Figure 2.19: a) Ideal class-F power amplifier and b) its waveforms at the output node

Conclusion

Linear modes PAs such as class –A, -B, - AB have high linearity performance and can be used to amplify a variable envelope signal without adding other linearization schemes. But those amplifiers have poor efficiency. Classes-C, -E and -F have very high potential to get high efficiency in RF frequencies but suffer from poor linearity. This illustrates the efficiency-linearity trade-off in traditional power amplifiers.

2.4 Efficiency Enhancement Techniques

This section describes some of the efficiency enhancement techniques that defy the traditional efficiency-linearity trade-off in power amplifiers. These techniques try to enhance the efficiency at low envelope power, thus increasing the average efficiency.

2.4.1 Doherty Amplifier

The Doherty technique [11], first proposed in 1936 for use in high-power broadcast transmitters, is the simplest efficiency boosting technique. The Doherty configuration

uses an active load-pull technique. The detail about the load-pull technique is explained in [12]. Figure 2.20(a) shows the schematic of the active load-pull technique. According to circuit theory, Gen1 sees the load resistance of R_L if Gen2 doesn't supply any current. When Gen2 starts to supply a current proportional to I_1, the resistance seen by the Gen1 will be: $R_1 = R_L\left(1+\frac{I_2}{I_1}\right)$

As I_2 increases, the resistance, R_1, seen by the Gen1 also increases. So the resistance seen by Gen1 can be modified according to the current supplied by the Gen2. Similarly, Gen2 sees a resistance of: $R_2 = R_L\left(1+\frac{I_1}{I_2}\right)$

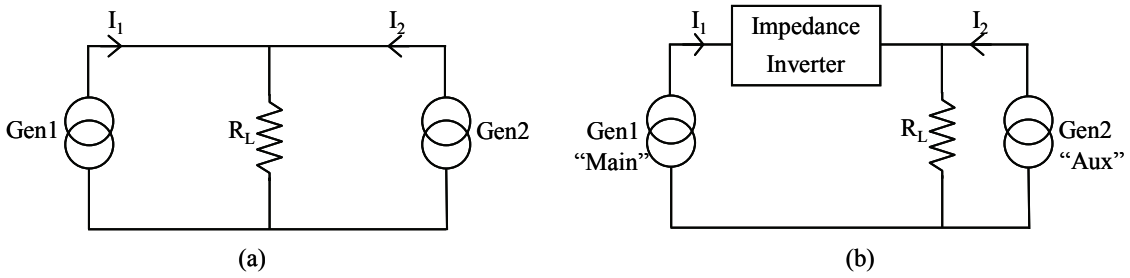


Figure 2.20: (a) Schematic of active load-pull technique (b) with impedance inverter illustrating the configuration of Doherty amplifier

Similarly in Figure 2.20(b), an impedance inverter is added so that the impedance seen by the Gen1 decreases as the current supplied by the Gen2 increases.

Operation of the Doherty Amplifier

The simplest configuration of a Doherty circuit (two-way) consists of two amplifiers; "main" or "carrier" amplifier and the "auxiliary" or "peaking" amplifier. The amplifiers are connected in parallel with a quarter wave transmission line (impedance inverter) as shown in Figure 2.21 so that the configuration is equivalent to Figure 2.20(b) with the Gen1 as the main and the Gen2 as the auxiliary amplifier.

The basic concept of the Doherty amplifier is to allow the main amplifier to operate at the maximum efficiency (peak power) while allowing the auxiliary amplifier to deal with the modulation peaks. When the input drive is low the auxiliary amplifier is shut-down and the main amplifier operates in the linear mode as shown in Figure 2.22. If a class-B PA is used as the main amplifier and the class-C as auxiliary amplifier, the class-C is off because signal is too small. As the input drive increases, the main amplifier starts to saturate and the auxiliary amplifier starts to supply current. This turn-on point of the auxiliary amplifier is called the ***transition point***. At the transition point, the efficiency of the overall system becomes high.

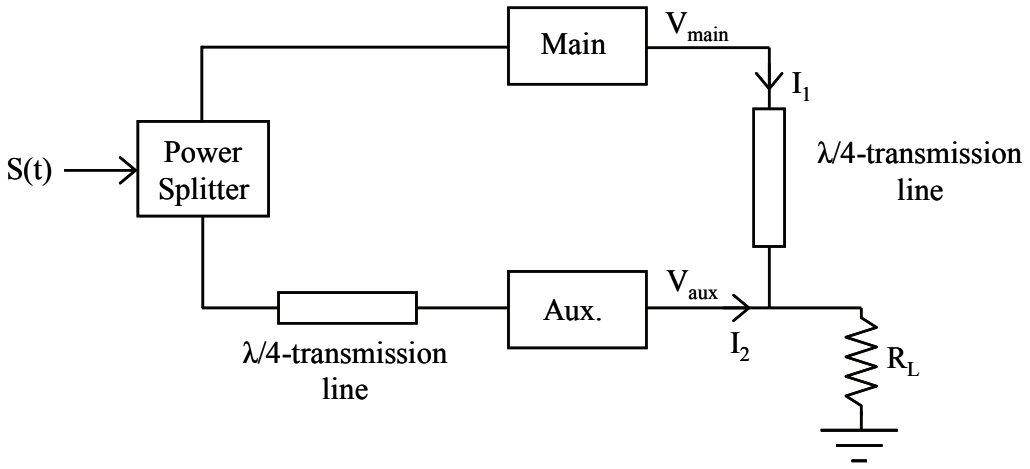


Figure 2.21: Schematic of Doherty Amplifier

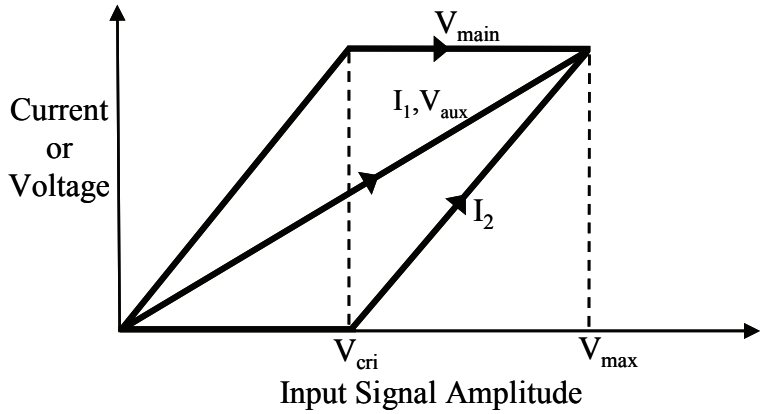


Figure 2.22: Current and Voltage at the output of the main and auxiliary amplifier

Above the transition point, the impedance seen by the main amplifier reduces due to the current supplied by the auxiliary amplifier. Because of this "load pulling" effect, the main amplifier delivers more current to the load and operates as a controlled voltage source while it is saturated. On the other hand, the auxiliary amplifier takes over operation as a linear amplifier. In this region both devices contribute to the output power. At the peak envelop power the auxiliary amplifier is also saturated and the efficiency of the overall system becomes again high. In this way, the two amplifiers give a composite linear power response, maintaining the efficiency close to maximum, typically down to the 6dB back-off point. (Note: typically for a two-way Doherty amplifier, the transition point is chosen at 6dB below the composite maximum power). Figure 2.22 shows the current and the voltage characteristic of the main and the auxiliary amplifier for the whole range of input voltages.

Performance of the Doherty Amplifier

The overall efficiency characteristic of the Doherty amplifier as a function of power back-off is shown in Figure 2.23.

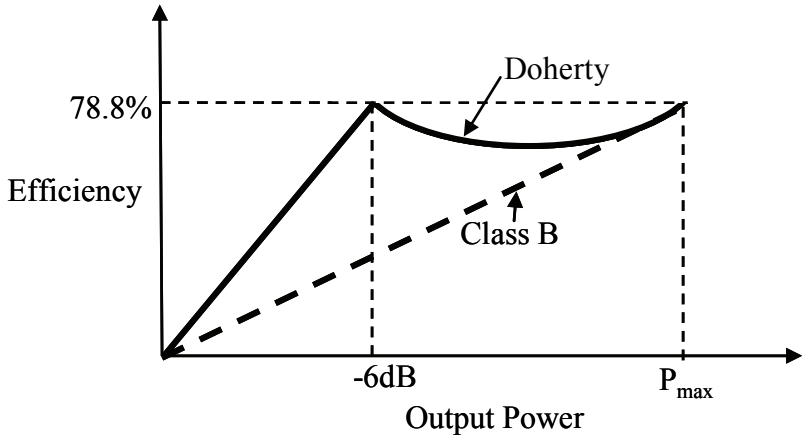


Figure 2.23 Efficiency versus power back-off of Doherty amplifier (solid line) and class-B amplifier (dotted line)

If a class-B PA is used as the main amplifier and the class-C as auxiliary amplifier, the theoretical maximum efficiency is 78.8%. The efficiency is close to the maximum throughout the upper 6dB. The small dip in the efficiency in between the transition point and full power (i.e. at 6dB back-off) is due to the lower efficiency of the auxiliary amplifier which operates in back back-off.

Disadvantages

A Doherty amplifier is very narrow band because of the use of quarter-wave transmission lines and the requirements of accurate phase matching between the two paths. Another drawback is the poor IMD performance mainly due to the low biasing of the auxiliary amplifier. However, other linearization scheme can be implemented to improve the linearity in the Doherty amplifier but this will add the complexity.

Region of operation	**Main Amplifier**	**Auxiliary amplifier**	**Overall Efficiency**
Below the transition point	Operates in linear mode	Shut down	poor
At the transition point	Just saturated	Just turn -on	maximum
Above the transition point and below the full power	Saturated	Operates in linear mode	Close to maximum
At Full Power	saturated	saturated	maximum

Table 2.1: Summary of the operation of the Doherty Amplifier

Improved Doherty Amplifier

Various techniques are employed to improve the performance of Doherty amplifiers. In [13], [14] envelop tracking is used to vary the bias point of the auxiliary amplifier according to the envelope of the input signal for high efficiency and linearity of the Doherty amplifier. Instead of choosing the transition point at 6dB back-off, [15] implemented the Doherty technique with the transition point at 10-dB back-off. To handle the large power back-off that means to amplify the variable envelope signal with large PAPR, the number of paths can be increased. The N-way Doherty amplifier is basically paralleling one carrier amplifier and N-1 numbers of auxiliary amplifiers. Two, three and four-way structure are implemented in [16], [17] which have the transition point at 6-, 10- and 12-dB output power back-off. Similarly one auxiliary amplifier and a number of main amplifiers can also be used; this structure is called the multi-stage Doherty amplifier. This configuration has two main advantages; i) the range of power back-off increases and ii)the overall efficiency characteristic of the Doherty system becomes close to ideal due to increase in the number of transition points, as the number of stages increases. This is shown in [5]. A Doherty amplifier with improved load matching using a load modulation technique is presented in [18].

Conclusion

Predominantly Class-A or -AB or -B is used as the "main" amplifier and class-C is used as the Auxiliary amplifier. However, switch mode PAs can also be used as the main [19] if the PER or exact possible power back-off is known and the transition point is chosen according to that. The performance of the Doherty topology mainly depends on the class of operation of the two amplifier blocks. Using the Doherty technique, the efficiency at back-off can be kept close to that in saturated condition.

2.4.2 Outphasing Amplifier

The Outphasing technique was first introduced in 1930s by Chireix. This technique is also named LINC (Linear Amplification Using Nonlinear Components), when it came into use at microwave frequencies in 1970's. In this technique, the envelope varying signal is first decoupled into two phasors with equal amplitudes. The phasors are then amplified separately in highly power efficient nonlinear amplifiers and finally the originally AM component is recovered by recombining those two signals.

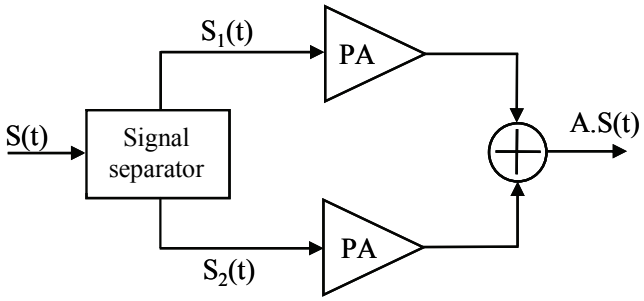


Figure 2.24 LINC PA block diagram

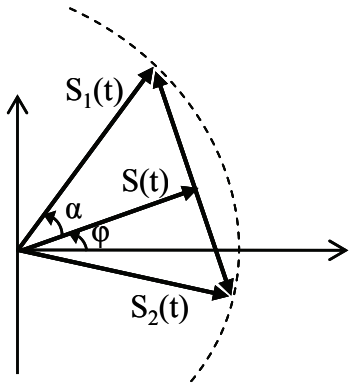


Figure 2.25 Vector diagram showing the input signal and the constant amplitude signals at the output of the signal separator

To understand this principle in more detail consider a variable envelope signal

$$S(t) = A(t)\cos(\omega_c t + \varphi) \tag{2.11}$$

As shown in Figure 2.25, this signal can decomposed into two signals having equal amplitude:

$$S_1(t) = \cos(\omega_c t + \varphi + \alpha) \tag{2.12}$$

and

$$S_2(t) = \cos(\omega_c t + \varphi - \alpha) \tag{2.13}$$

Such that

$$2S(t) = S_1(t) + S_2(t) \tag{2.14}$$

Where
$\alpha = \cos^{-1}[A(t)]$

The key elements in the outphasing PAs are the phase modulator (signal separator) and the output power combiner. The signal separator decomposes the incoming signal vector (S(t)) of any magnitude and phase into two vectors ($S_1(t)$ and $S_2(t)$) with constant magnitude. A DSP is assumed to be the best choice for signal component separation. However, an analog signal component separator is also promising [20]. After amplification the two signals are added by using the output power combiner.

As the outputs of the PAs in the two paths are about to phase cancel in order to generate a low amplitude output, the dc power drawn by the pair of the saturated PA is also reduced because of the increase in equivalent load resistance seen by each device. This load pulling effect preserves the high efficiency during low amplitude input. This is the key feature of out-phasing PAs.

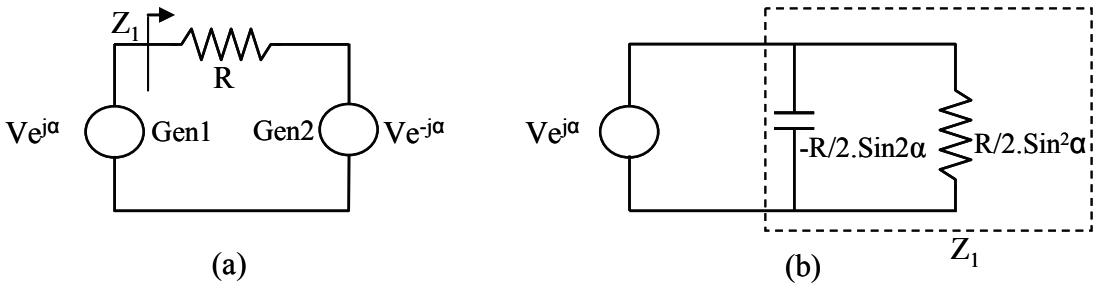


Figure 2.26: a) Output schematic of out-phasing amplifier, b) Equivalent circuit at generator 1

Figure 2.26(a) shows the schematic of a possible RF output connection and Figure 2.26(b) shows the equivalent load seen by the Gen 1 due to the effect of the out-phasing modulation. It can be clearly seen that the phase difference between the two generators is causing a reactive component at the load. As α increase towards 45° to reduce the output envelope amplitude, the load seen by the generator becomes more reactive, causing lower efficiency. Chireix proposed the use of an additional reactive component across the devices to compensate the out-phasing reactance. However, the compensation can be done at only one value of the phase angle φ and of course the efficiency is again the maximum at this point.

Disadvantages

- To achieve potentially high efficiency, it is desirable to use switch-mode power amplifiers such as class-E for the implementation of the component amplifiers. Unfortunately, the class-E PA is not well-suited for outphasing system because of varying load impedance with lossless power combining [21], [22]. The zero voltage switching characteristic is only valid for the fixed load. So, the class-E power amplifiers are best suited with lossy power combiner such as Wilkinson combiner that provides the isolation between the amplifiers output with fixed input impedance. However the power combining is inevitably lossy as only the fraction of the output power of class-E appears at the combiner output and the rests is dissipated across the combiner's resistor, depending on the relative phase of the amplifiers.

  Interestingly, class-D amplifier is attractive for outphasing implementation [21]. In the class-D case, when the phase of the load current is different than that of the voltage, there is a positive and negative current flow through the switches. So, the current is drawn from the supply and return back to it in the same cycle through the high-side switch. For a phase difference of 90° between the load current and voltage, which means for zero output power of the outphasing system, the average current drawn from the supply is zero. This is an attractive property to achieve high efficiency at low output power. However, the class-D amplifier suffers from high switching loss from its output capacitance for high frequency applications.

- The output power is extremely sensitive to the out-phasing angle especially for low output amplitude and hence the phase mismatch between the two paths (in some cases 1^o of out-phasing angle could result -40dB variation in the output power [12]). So this technique is not so suitable when a large back-off is needed. Consequently, this technique is best suited for a modulation scheme that avoids zero crossing like $\pi/4$-shifted-DQPSK.

- Signal separation is complex

Conclusion

Reactive compensation is the key element to improve the average efficiency of an out-phasing PA. But even without reactive compensation the efficiency characteristic is attractive. An out-phasing technique using DSP phase control in baseband (LINC transmitter) is popular in linear applications. Due to the high sensitivity to the phase imbalances, this technique is not so suitable for signals with high peak-to-average power ratio.

2.4.3 Adaptive Bias

The adaptive bias technique was primarily proposed to increase the power added efficiency of class-A amplifiers during large back-off. In this technique the bias level of the amplifier is varied with the envelop level to reduce the amount of dc current drawn from the supply during back-off. The operation of the adaptive bias scheme is shown in Figure 2.27. The gate bias of the PA is varied proportionally to the signal from the envelope detector.

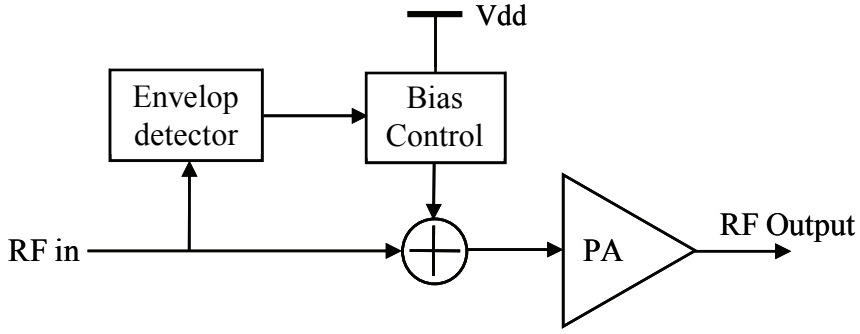


Figure 2.27: Schematic of the adaptive bias control

2.4.4 Envelope Elimination and Restoration or Polar Modulation

The Envelop Elimination and Restoration (EER) technique [23] was first proposed by Kahn in 1952 and also known as Polar modulation technique. In its classic structure as shown in Figure 2.28, the amplitude and phase information are separated from the input signal using an envelope detector and a limiter. The phase modulated signal is then amplified by a highly efficient amplifier such as class-C, -D, -E, or -F. The envelope

(amplitude information) is used to modulate the power supply of the final RF PA to restore the signal envelope at the output.

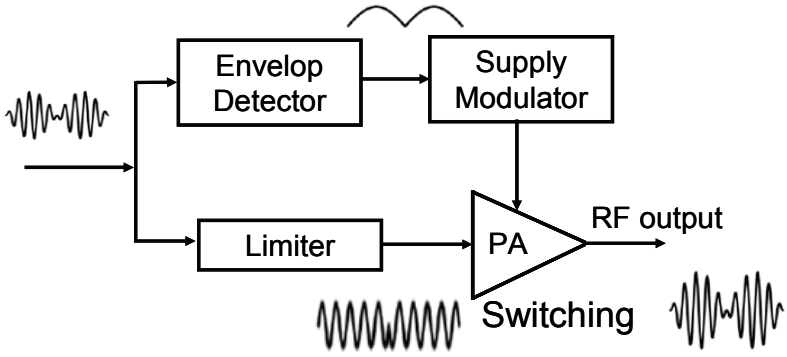


Figure 2.28: Schematic of EER/Polar modulation technique

Since switch mode amplifiers can be used both in the supply modulator as well as in the final power amplifier, this technique has a potential to achieve high efficiency, theoretically 100%. Details about this technique will be discussed in chapter IV.

2.4.5 Envelope Tracking

The absence of a limiter before the RF PA is the main difference between an Envelope Tracking (ET) and the EER architecture. As a result, the RF drive contains both the amplitude and the phase information and the burden of linearity lies on the RF PA itself. This technique is also called "dynamic drain/collector biasing".

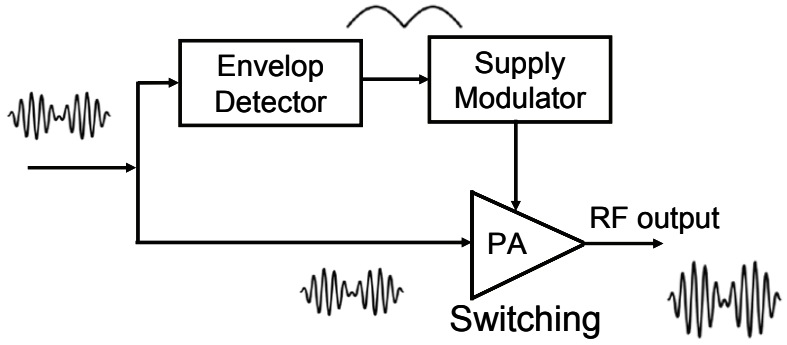


Figure 2.29: ***Envelope tracking architecture***

As shown in Figure 2.29, the envelope detector extracts the envelope information from the RF input signal and uses it to control the collector/drain voltage of the PA through a supply modulator. The supply modulator dynamically adjusts the RF PA with just sufficient supply voltage to reduce the dc power consumption at low power levels, thus increasing the average efficiency of the whole system. Other advantage is that the linearity of the system is less dependent on the bandwidth of the supply modulator. In

summary this technique is much simpler to implement than an EER, where each block has tough requirements.

Some disadvantages of Envelope tracking techniques are:

- The theoretical maximum average efficiency is not as high as for the EER technique because of the use of a linear mode PA. Average efficiency is directly proportional to the peak to average power ratio.
- Mismatch of the delays between the two paths (supply and signal paths) degrades the linearity, though not as much as with EER.
- The power gain of the PA decreases as the supply voltage is reduced.

2.4.6 Summary of Efficiency Boosting Techniques

Various efficiency boosting techniques were summarized in this section. The Doherty technique is based on an active load-pull technique. Basically, the efficiency boosting techniques described above are mainly based on "load pulling" and "Vdd pulling" so that the output of the PA swings from rail-to-rail. The Doherty and Chierex techniques use load pulling while ET and EER are based on Vdd pulling.

The basic concept of the Doherty amplifier is to allow the main amplifier to operate at the maximum efficiency (peak power) while allowing the auxiliary amplifier to deal with the modulation peaks. So the overall efficiency remains high during back-off as well. The Chierex/LINC architecture has the exciting feature that it first divides the varying envelope signal into two constant envelope signals which are then amplified by highly efficient non-linear amplifiers. However, the signal separation and the recombination after amplification are a difficult task. The Envelope Elimination and Restoration technique was also briefly discussed in this chapter. The main feature of this technique is the theoretical 100% efficiency regardless of the power back-off. Each block in the EER topology has strict requirements to satisfy the linearity of the overall PA system. A less aggressive technique is Envelope Tracking. In ET, the burden of linearity lies on the final PA itself. So the final PA must be a linear PA and hence the average efficiency is not as high as the EER technique.

2.5 Output Filtering

No matter which kind of amplifier is used, filters at the output are considered inevitable to suppress the harmonic products generated by non-linearities. Suppression of the harmonics avoids signal interference with other devices operating in a different frequency band. The output matching network of a power amplifier attenuates the harmonics significantly depending on the type and configuration as it is mostly narrowband. So the matching network itself acts as a filter. A separate RF filter after the matching network might also be needed to further suppress the harmonics. Nevertheless, the output filter (matching network and the additional filter if present) in all wireless transmitters has to make sure that the harmonics are suppressed to the acceptable level.

Main consequence of the output filtering is that dedicated hardware or filters are needed for each standard. Nonetheless, in a typical multi-standard transmitter, with multiple narrow-band power amplifiers which are limited in bandwidth by dedicated filters, each standard can have its own antenna or can be made selectable by a switch. With the ever increasing number of different standards to be supported, this architecture becomes increasingly unpractical and not an economical solution, as support for every new frequency band requires adding external dedicated components. So in future mobile communications, a flexible hardware is desired that can be used for different standards under software control. Such flexibility is envisioned in software-defined radio and cognitive radio system. One way to achieve this is to use tunable filters. In [24], [25], [26], [27], a Micro-Electro-Mechanical-Systems (MEMS) switch is used to tune the filter to different frequency band. MEMS switches are an attractive option since they have high power handling capability and low insertion loss. However, it needs an especial packaging because MEMS switches are moving devices that are vulnerable to contamination from various environmental sources such as dust, moistures and gas vapors. This results in increase cost and size [28]. A circuit employing MEMS devices often reaches dozens or hundreds of square millimeters [24]. Furthermore, MEMS switch needs high excitation voltage (about 50V) which is not available in mobile phones and the 10 years life time reliability has not yet been proven for low cost MEMS solutions [28].

Another way to solve the problem of output filtering, one major stumbling block towards implementing flexible radio transmitter, is to relax or even completely eliminate the bulky filter by canceling harmonics and sidebands generated by the nonlinear circuits. For the matching, a wideband matching network in the form of transformer or lumped elements [29], [30], [31] can be used. In the next chapter, a much more flexible architecture will be discussed as shown in Figure 3.1(b): one wideband integrated power upconverter with no dedicated external filters will be discussed. The polyphase multipath circuit theory proposed in [32] is used to generate a clean output spectrum by canceling a very large multitude of harmonics and sidebands.

2.6 Summary and Conclusions

To design a power amplifier for digital wireless communication standards that uses spectrally efficient complex modulation schemes and multiple carriers, the understanding of the characteristics of the digital signal is necessary to optimize the power amplifier's performance in terms of both linearity and efficiency. There are different ways to measure the linearity and the efficiency. Spectral mask, EVM, ACPR, NPR measurements are used to specify the linearity of the transmitter. The most convincing method to measure the efficiency performance of the power amplifier, used to amplify the variable envelope signal, is the average efficiency as it directly relates to the battery life time.

A trade-off between linearity and efficiency always exists in classic power amplifiers. Linear mode PAs like class-A and class-AB are good for linearity and switch mode PAs like class-E and class-F are good for efficiency. Doherty, LINC, Envelop tracking and

Polar Modulation techniques are known to enhance the efficiency of the power amplifiers, overcoming that trade-off.

Filtering at the output is needed to suppress the harmonics generated by the non-linearity of the power amplifier to acceptable levels as defined by the concerned regulatory bodies. The consequence of the presence of fixed frequency filters is that the resulting transmitter hardware is inflexible.

References:

[1] X. Zhang, L.E. Larson and P.M. Asbeck, "Design of Linear RF Outphasing Power Amplifiers", Artech House, 2003

[2] W. Webb, "The Complete Wireless Communications Professional: A Guide for Engineers and Managers", Artech House, 1999

[3] C. Langton, "All about modulation: Part-I", (online):http://people.seas.harvard.edu/ ~jones/ cscie129/papers/modulation_1.pdf

[4] Wireless LAN and Medium Access Control (MAC) and Physical Layer (PHY) Specifications: High-speed Physical Layer in the 5GHz Band, IEEE Std. 802.11a-1999

[5] P. Kenington, "High-Linearity RF Amplifier Design", Artech House, 2000

[6] J. B. Groe and L. E. Larson, "CDMA Mobile Radio Design", Artech House, 2000

[7] D.M. Albulet, "RF Power Amplifiers" Noble Publishing, Atlanta, 2001

[8] F.H. Raab, P. Asbeck, S. Cripps, P.B. Kenington, Z.B. Popovic, N. Pothecary, J.F. Sevic, and N.O. Sokal, "Power amplifiers and transmitters for RF and microwave", *IEEE Transactions on Microwave Theory and Techniques*, Volume: 50, Issue: 3, March 2002

[9] R.S. Narayanaswami, "RF CMOS Class C Power Amplifiers for Wireless Communications", *Ph.D. Thesis*, December 2001

[10] N.O. Sokal and A.D. Sokal, "Class E—A new class of high-efficiency tuned single-ended switching power amplifiers", *IEEE Journal of Solid-State Circuit-10*, pp 168–176, June 1975

[11] W.H. Doherty, "A new high efficiency power amplifier for modulated waves", *Proc. IRE*, Vol. 24, No. 9, pp-1163-1182, September 1936

[12] S. Cripps, "RF Power Amplifiers for Wireless communications", Artech House, 1999

[13] Y. Yang, J. Cha, B. Shin, and B. Kim, "A microwave Doherty amplifier employing envelope tracking technique for high efficiency and linearity", *IEEE Microwave and Wireless Components Letters*, v 13, n 9, September 2003

[14] J. Moon, J. Kim, I. Kim, J. Kim, and B. Kim, "A Wideband Envelope Tracking Doherty Amplifier for WiMAX Systems", *IEEE Microwave and Wireless Components Letters*, Vol. 18, No. 1, January 2008

[15] M. Iwamoto, A. Williams, P. Chen, A.G. Metzger, L.E. Larson, and P.M. Asbeck, "An extended Doherty amplifier with high efficiency over a wide power range", *IEEE Transactions on Microwave Theory and Techniques*, v 49, n 12, December 2001

[16] Y. Yang, J. Cha, B. Shin, and B. Kim, "A fully matched N-way Doherty amplifier with optimized linearity", *IEEE Transactions on Microwave Theory and Techniques*, v 51, n 3, March 2003

[17] J. Moon, J. Kim, I. Kim, J. Kim, and B. Kim, "Highly Efficient Three-Way Saturated Doherty Amplifier With Digital Feedback Predistortion", *IEEE Microwave and Wireless Components Letters*, Vol. 18, No. 8, August 2008

[18] Y. Yang, J. Yi, Y.Y Woo, B. Kim, J. Nam and J. Cha, "Efficiency Enhancement of linear power amplifier using load modulation technique", *International symposium on Microwave Optical Technology Dig.*, pp. 505-508, June 2001

[19] Y. Suzuki, T. Hirota, and T. Nojima, "Highly efficient feed-forward amplifier using a Class-F Doherty amplifier", *IEEE MTT-S International Microwave Symposium Digest* (Cat. No.03CH37411), pt. 1, p 77-80 vol.1, 2003

[20] B. Shi and L. Sundstrom, "A 200-MHz IF BiCMOS signal component separator for linear LINC transmitters", *IEEE Journal of Solid-State Circuits*, v 35, n 7, p 987-93, July 2000

[21] X. Zhang, L.E. Larson and P.M. Asbeck, "Design of linear RF outphasing power amplifiers ", Artech House, 2003

[22] A.D. Pham, "Outphase Power Amplifiers in OFDM Systems", *Ph.D. Thesis*, Massachusetts Institute of Technology, 2005

[23] L.R. Kahn, "Single-sideband transmission by envelope elimination and restoration", *Proc. IRE*, pp. 803–806, July 1952

[24] H. Okazaki, A. Fukuda, K. Kawai, T. Furuta, and S. Narahashi, "MEMS-based Reconfigurable RF Front-end Architecture for Future Band-free Mobile Terminals", *Proceedings of the 37th European Microwave Conference*, pp. 1058-1061, October 2007

[25] A. Fukuda, T. Furuta, H. Okazaki, and S. Narahashi, “A 0.9-5-GHz wide-range 1W-class reconfigurable power amplifier employing RFMEMS switches”, in *2006 IEEE MTT-S International Microwave Symposium Digest*, pp. 1859–1862, June 2006

[26] H. Okazaki, A. Fukuda, K. Kawai, T. Furuta, and S. Narahashi, “Reconfigurable RF Circuits for Future Band-Free Mobile Terminals”, *International Symposium on Signals, Systems and Electronics*, August 2007

[27] L. Larcher, R. Brama, M. Ganzerli, J Iannacci, B. Margesin, M. Bedani and A. Gnudi, “A MEMS Reconfigurable Quad-band Class-E Power Amplifier for GSM Standard”, *IEEE 22nd International Conference on MEMS*, pp. 864-867, January 2009

[28] R. Jones and M. Chapman, “RF MEMS in mobile phones”, accessible via www.rfdesign.com, 2005

[29] Y.E. Chen, L. Yang, and W. Yeh, “An Integrated Wideband Power Amplifier for Cognitive Radio”, *IEEE Transactions on Microwave Theory and Techniques*. Vol. 55, No.10, pp. 2053-2058, October 2007

[30] S. Kousai, A. Hajimiri, “An Octave-Range Watt-Level Fully Integrated CMOS Switching Power Mixer Array for Linearization and Back-Off Efficiency Improvement”, *ISSCC Digest of Technical Papers*, February 2009

[31] F.M.A. Al-Raie, “A systematic technique for designing wideband RF power amplifiers”, *International RF and Microwave Circuit Conference proceedings*, September 2006

[32] R. Shrestha, E. Mensink, E.A.M. Klumperink, G. J. M. Wienk, and B. Nauta, "A Polyphase Multipath Technique for software-defined radio transmitters", *IEEE Journal of Solid State Circuits*, Vol. 41, pp.2681-2692, December 2006

Chapter 3

Wideband Power Upconverter for Software Defined Radios

One of the biggest challenges in implementing flexible or reconfigurable radio transmitter for Software Defined Radio is the presence of a fixed frequency output filter. One way to solve this problem is by canceling harmonics and sidebands generated by a nonlinear circuit so that there is no need for the fixed frequency output filter. For reasons of cost and form factor, this solution which can be fully integrated in CMOS is preferred compared to other solutions like MEMS based reconfigurable filters, and the use of multiple filters and switches.

A recent step in this direction is the harmonic rejection mixer canceling the third and fifth harmonics [1], thus relaxing analog filter requirements. The same technique is also used for cognitive radio applications in [2] to realize a CMOS direct upconversion transmitter. However the tunable filters are still needed to suppress 7^{th} or higher harmonics though its requirements are relaxed. In a mixer-DAC [3], the zero-order hold filtering is used to reduce DAC related spurs. However, this approach doesn't address the problem of mixer harmonics around odd LO-harmonics, caused by multiplication with a square-wave LO-signal (hard switching mixer). A reconfigurable FIR band-pass filtering through a passive power combiner is proposed in [4] to replace the zero-order hold filter. However, it needs a separate passive technology to realize the power combiner.

In this chapter, we exploit the polyphase multipath circuit theory proposed in [5], to further reduce or even completely eliminate bulky filters by canceling a very large multitude of harmonics and sidebands. We apply the technique to realize a wideband *filter-less* power upconverter [6], [7] for software defined radio transmitter applications, using only digital circuits and switched transconductor mixers [8]. We mainly focus on a proof-of-concept of the polyphase multipath technique and do not aim for any particular standard.

The chapter is organized as follows: in Section 3.1, the principle behind the rejection of harmonics and sidebands using the polyphase multipath technique is explained. The use of a mixer as phase shifter is discussed in Section 3.2. An implementation of the technique aiming at a filter-less power upconverter is described in Section 3.3. The circuit implementation and various design considerations are explained in Section 3.4. Measurement results are presented in Section 3.5, and conclusions are drawn in Section 3.6.

3.1 Polyphase Multipath Technique

3.1.1 Basic Principle of Harmonic Cancellation

Mathematically, the input/output characteristics of a memory less non-linear system can be represented by a power series expansion as given below.

$$y(t) = a_0 + a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) + ... \quad 3.1$$

Where x(t) is an input signal applied to a non-linear system and y(t) is the resulting output. Coefficient a_0 represents the DC-offset and a_1 is the linear component of the output. Similarly, a_2, a_3 are the coefficients related to nonlinearities and represent second and third order nonlinearities respectively and so on. The values of these coefficients are dependent on the characteristic of the nonlinear system. If a nonlinear circuit modeled as in equation 3.1 is excited by a sinusoidal signal Acos(ωt), the output contain a wanted output signal at ω but also unwanted harmonic distortion at 2ω, 3ω, 4ω, etc. and can be written as:

$$y(t) = b_0 + b_1 \cos(\omega t) + b_2 \cos(2\omega t) + b_3 \cos(3\omega t) + ... \quad 3.2$$

Where $b_0 = a_0 + \frac{a_2 A^2}{2} + ...,\ b_1 = a_1 A + \frac{3a_3 A^3}{4} + ...,\ b_2 = \frac{a_2 A^2}{2} + ...,\ b_3 = \frac{a_3 A^3}{4} + ...$

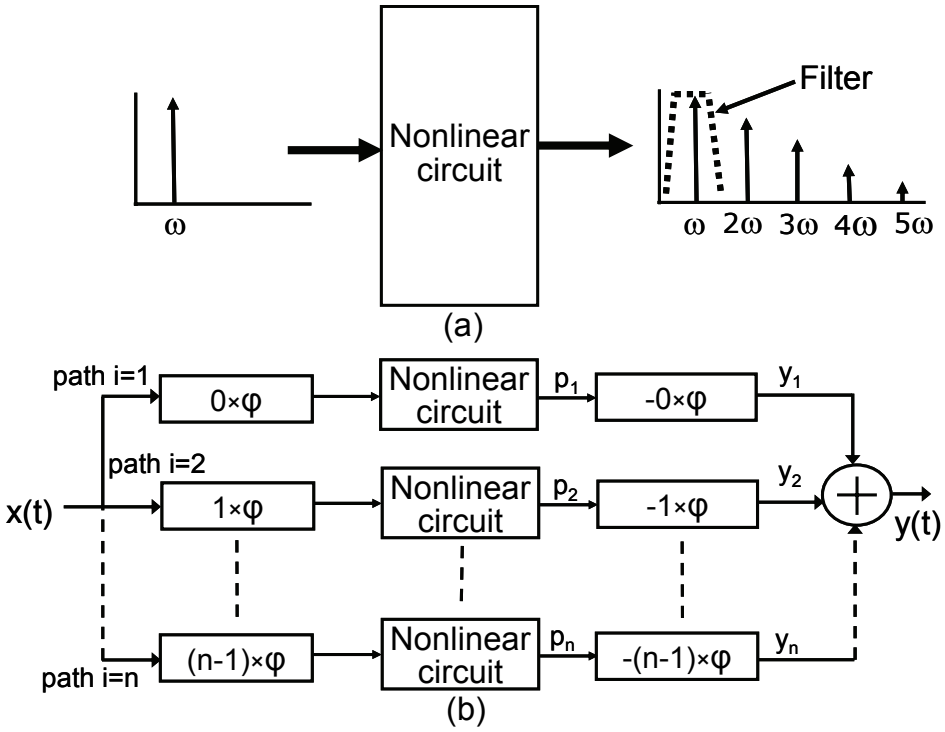


Figure 3.1: (a) A nonlinear circuit (1-path) (b) Polyphase n-path circuit

Figure 3.1(b) shows a polyphase n-path circuit, cancelling many harmonics of ω [5]. The basic idea is to divide the nonlinear circuit in Figure 3.1(a) into 'n' equal smaller pieces, and apply an equal but opposite phase shift before and after each nonlinear circuit. If the phase shift in path 'i' is (i-1)×φ, where φ is a phase shift constant satisfying n×φ=360°, the circuit will produce the same wanted harmonic as Figure 3.1(a), but cancel many higher harmonics. Mathematically this can be shown using a power series expansion, assuming a memory-less weakly non-linear system. If the signal x(t) = Acos(ωt) is applied to the input as shown in Figure 3.1(b), the output of the *nonlinear circuit* of the i^{th} path can be written as,

$$p_i(t) = b_0 + b_1\cos(\omega t + (i-1)\varphi) + b_2\cos(2\omega t + 2(i-1)\varphi) + b_3\cos(3\omega t + 3(i-1)\varphi) + \ldots \qquad 3.3$$

Where b_0, b_1, b_2, b_3…. are Taylor series constants characterizing the nonlinearity [9] as in equation 3.1. From equation 3.3, it can be seen that the phase of the 'k^{th}' harmonic at the output of the nonlinear circuit rotates by 'k' times the input phase (i-1)φ. The phase shifters, -(i-1)φ, after the nonlinear blocks are required to align the fundamental components at ω in phase again. The phase sequence of the phase shifters before and after the non-linear component should be opposite to get the fundamental component in the phase. So, it will not be cancelled but the higher order harmonics will still have the different phases.

The signals at the output of these phase shifters in the i^{th} path can be written as:

$$y_i(t) = b_0 + b_1\cos(\omega t) + b_2\cos(2\omega t + (i-1)\varphi) + b_3\cos(3\omega t + 2(i-1)\varphi) + \ldots\ldots \quad 3.4$$

In equation 3.4, the phase of the fundamental component is identical for all the paths, but the phases of the harmonics are different for each path. The fundamental components are added up when the outputs of all paths are added. If the phase φ is chosen such that $\varphi = 360^o/n$, then all the higher harmonics are cancelled [5], except for the k^{th} harmonics for which:

$$k = j\times n + 1 \qquad \text{where } j=0, 1, 2, 3, \ldots.. \quad 3.5$$

In general, if 'k' is the order of the harmonics, then the phase shift of the k^{th} harmonics at the output of i^{th} path will be $i\times\varphi\times(k-1)$ as shown in Figure 3.1(a). For $k\neq(j\times n+1)$, the summation of k^{th} harmonics at the output of each path y_i creates a balanced structure and hence they are cancelled. But the $(j\times n+1)^{th}$ harmonics always have the same phase at the output so they are not cancelled.

Mathematically, the summation of the signals at the output of all paths can be written as:

$$y(t) = nb_0 + nb_1\cos(\omega t) + b_2\sum_{i=1}^{n}\cos(2\omega t + (i-1)\varphi) + b_3\sum_{i=1}^{n}\cos(3\omega t + 2(i-1)\varphi) + \ldots\ldots \quad 3.6$$

From the phasor balance of vectors

$$\sum_{i=1}^{n}\cos(k\omega t + (k-1)(i-1)\varphi) = 0 \qquad \text{for } k\neq(j\times n+1)\ldots\ldots \quad 3.7$$

From equation 3.7, depending on the number of paths, the harmonics terms in the equation 3.1 are cancelled except for $k = (j\times n+1)$. So the obtained output is given by

$$y(t) = nb_0 + nb_1\cos(\omega t) + b_{n+1}\sum_{i=1}^{n}\cos((n+1)\omega t) + \ldots\ldots \quad 3.8$$

If the number of paths is sufficiently large such that the $(n+1)^{th}$ harmonics are weak at the output then the equation 3.8 contains only the dc and linear term. To illustrate the employed principle of harmonics cancellation, two examples are presented in the next sub-section.

3.1.2 Polyphase 2-path and 3-path circuit examples

Figure 3.2 shows a polyphase 2-path circuit which is nothing but a well-known differential circuit driven with balanced (anti-phase) input signals. Since the upper path

has a phase shift of 0°, all the harmonics generated by the nonlinear block as well as the fundamental component will have a phase of 0° at the output of the nonlinear block. In the lower path, the input of the nonlinear block has an opposite phase i.e. 180°. At the output the harmonics that are created by even power terms have a phase of 0° while the odd powers have a phase of 180°. This difference in phase is exploited to cancel the even harmonics by providing a phase of -180° to the lower path and then adding. At the output the fundamental and the odd harmonics arrive in phase so add up while the even harmonics arrive in anti-phase and are cancelled.

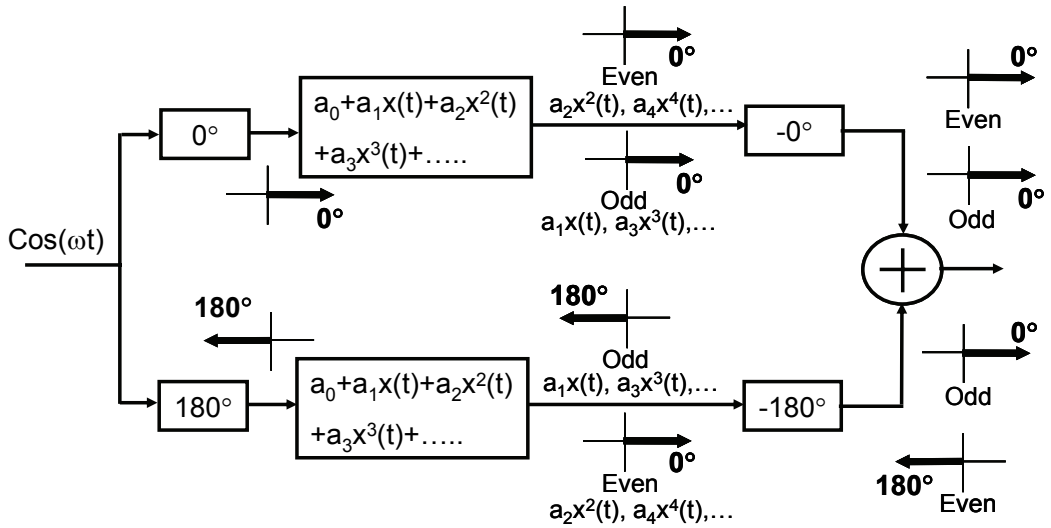


Figure 3.2: Polyphase 2-path circuit cancelling even order harmonics

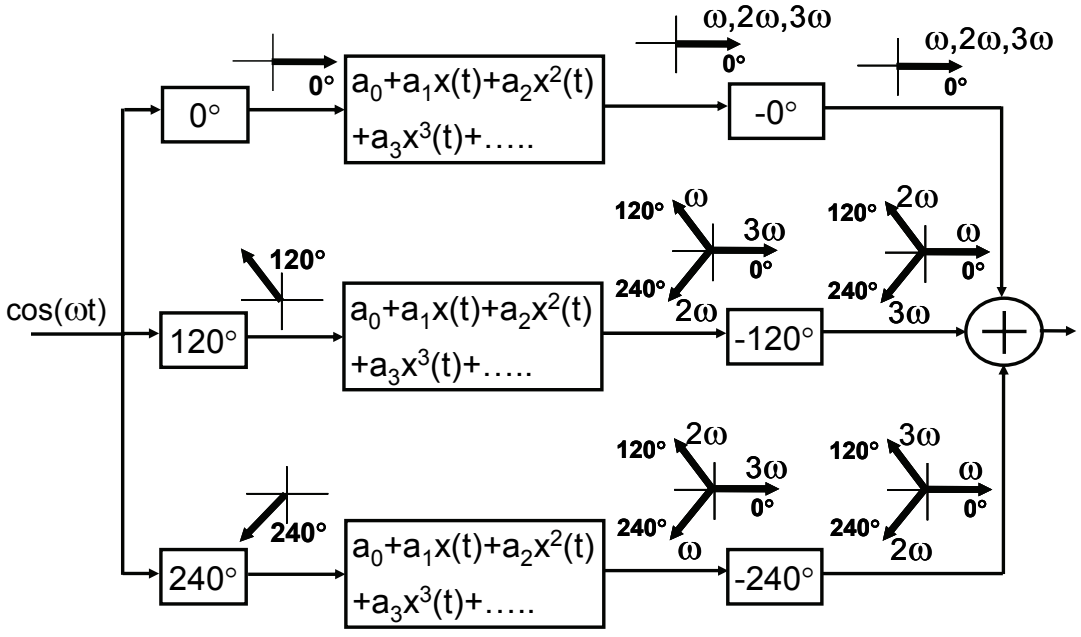


Figure 3.3: Polyphase 3-path circuit cancelling 2ω and 3ω harmonics

A system with three paths is shown in Figure 3.3. In this case, phase shifts of 0°, 120° and 240° are added before the nonlinear circuit to paths 1, 2 and 3 respectively, and equal but opposite phases -0°, -120° and -240° behind the block. Due to the nonlinearity, the phase rotation for the k^{th} harmonic is k times the input phase, so the fundamental component, the second harmonic and the third harmonic will have phase shifts of [0°, 0°, 0°], [0°, 120°, 240°] and [0°, 240°, 120°] respectively at the output of the nonlinear blocks of path 1, 2 and 3. The mathematical illustration of this is given in Appendix A. Figure 3.4(a) shows how the phases of the harmonics at the output of each path combine. The fundamental components add up in phase, while the vectors for the second and third harmonics create a "balanced structure" at the output, resulting in a zero sum (cancellation). However, the fourth harmonic components align in phase again, and will add up like the fundamental. Figure 3.4(b) shows that the 2^{nd}, 3^{rd}, 5^{th}, 6^{th} etc harmonics are cancelled and the first non-cancelled is the fourth with a 3-path system. Similarly for a 4-path system the first non-cancelled harmonic will be the fifth harmonic and in general for the n-path system the $(n+1)^{th}$ harmonic is the first non-cancelled harmonic. In other words, the higher the number of paths, the higher will be the number of harmonic cancellations. Theoretically, an infinite number of paths are needed to cancel all the harmonics. However, in practice higher order harmonics are weaker than low order harmonics and need not all be cancelled. Also, some filtering will in practice always be present, e.g. due to the limited bandwidth of an antenna or the speed limitations in a circuit. Moreover mismatches will put a practical limit on what is feasible (see section 3.4.4).

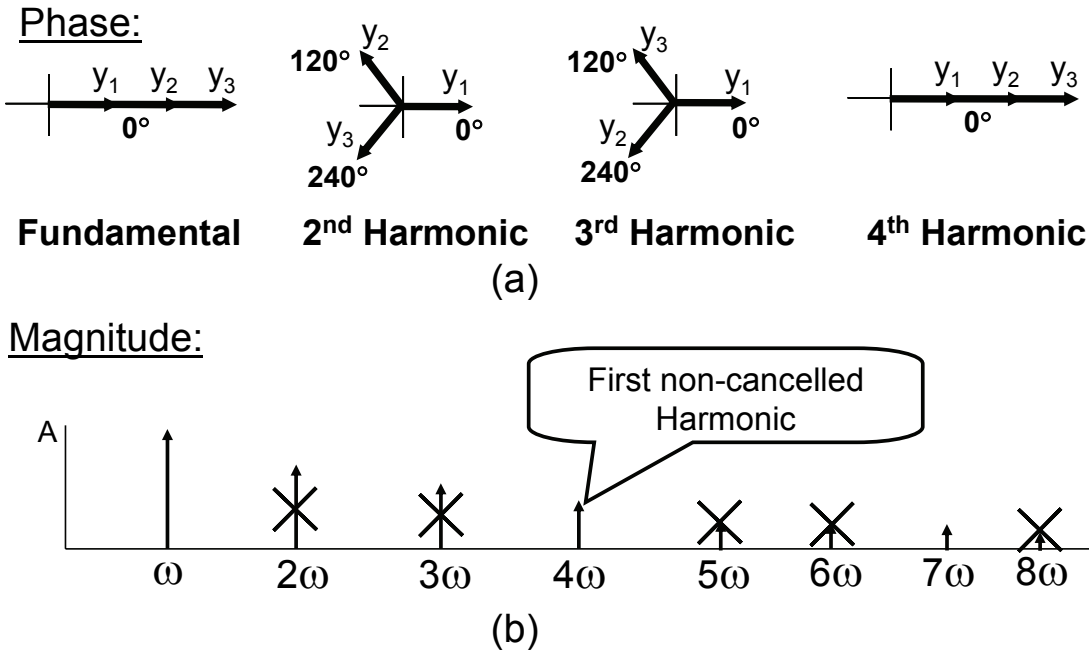


Figure 3.4: Output of the 3-path circuit in Fig. 4: (a) phasor diagrams and (b) spectral plot.

3.1.3 Generalization to intermodulation distortion

If the non-linear system as described in Figure 3.1(a) is excited by a two tone input signal $x(t) = A_1\cos\omega_1 t + A_2\cos\omega_2 t$, besides harmonics the output will also contain intermodulation products at new frequencies $\omega = p\omega_1 + q\omega_2$, where p and q identify harmonics of ω_1 and ω_2 respectively and can be positive or negative integer numbers. It is interesting to see whether the multipath technique also cancels such intermodulation products. To examine this, the phase relationship with the input frequency is important. In Figure 3.1(b), the phase shift of the k^{th} harmonic at the output of the i^{th} path is $(k-1)(i-1)\varphi$ for a single tone test. Similarly, in case of two tones, the phase shift of the $p\omega_1+q\omega_2$ products at the output of the i^{th} path will be $(p+q-1)(i-1)\varphi$. So the products which satisfy equation 3.9 will not be cancelled.

$$p+q = j\times n + 1 \quad \text{where } j=0, 1, 2, 3, \ldots \qquad 3.9$$

In particular, the third order intermodulation products ($2\omega_1-\omega_2$ and $2\omega_2-\omega_1$) satisfy equation 3.9 for j=0 because p+q=1. These products always appear in phase at the output of each path and hence they are not cancelled with the multipath technique. However other intermodulation products can be cancelled. In general, if p+q=k and the k^{th} harmonic is cancelled, then also $p\omega_1+q\omega_2$ is cancelled.

3.1.4 Conclusion

The polyphase multipath technique cancels the harmonics produced by the non-linearity of the system. The higher the number of paths, the higher will be the number of harmonic cancellations.

3.1.5 Discussion

In order to make a comparison, we look at the existing harmonic rejection technique [1] applied in a mixer. The mixer is called harmonic rejection mixer (HRM). The principle used for harmonic rejection is to generate an amplitude quantized sinusoid, $f_{LO}(t)$. In Figure 3.5(a) three-square waves; $x_1(t)$, $x_2(t)$ and $x_3(t)$ having the phase shift of 0^o, 45^o and 90^o at frequency ω_{LO} are summed to generate $x_{LO}(t)$. To exactly cancel the 3^{rd} and 5^{th} harmonics of the square wave, the magnitude of $x_2(t)$ is multiplied by $\sqrt{2}$.

The implementation of the technique in [1] is as shown in Figure 3.5(b). The three mixers are used in the three paths. The square wave in the 1^{st} , 2^{nd} and 3^{rd} paths, which are shifted by a phase of 0°,45° and 90° respectively, are mixed with a baseband signal at frequency ω_{BB}. Since the third and fifth harmonics of a squarewave have a phase shift of three and five times respectively the phase shift of the fundamental and the middle mixer is scaled by $\sqrt{2}$ times, the resultant of the third and fifth harmonic components at the output of the mixer are zero as shown in Figure 3.5(c). However, the fundamental components are added up.

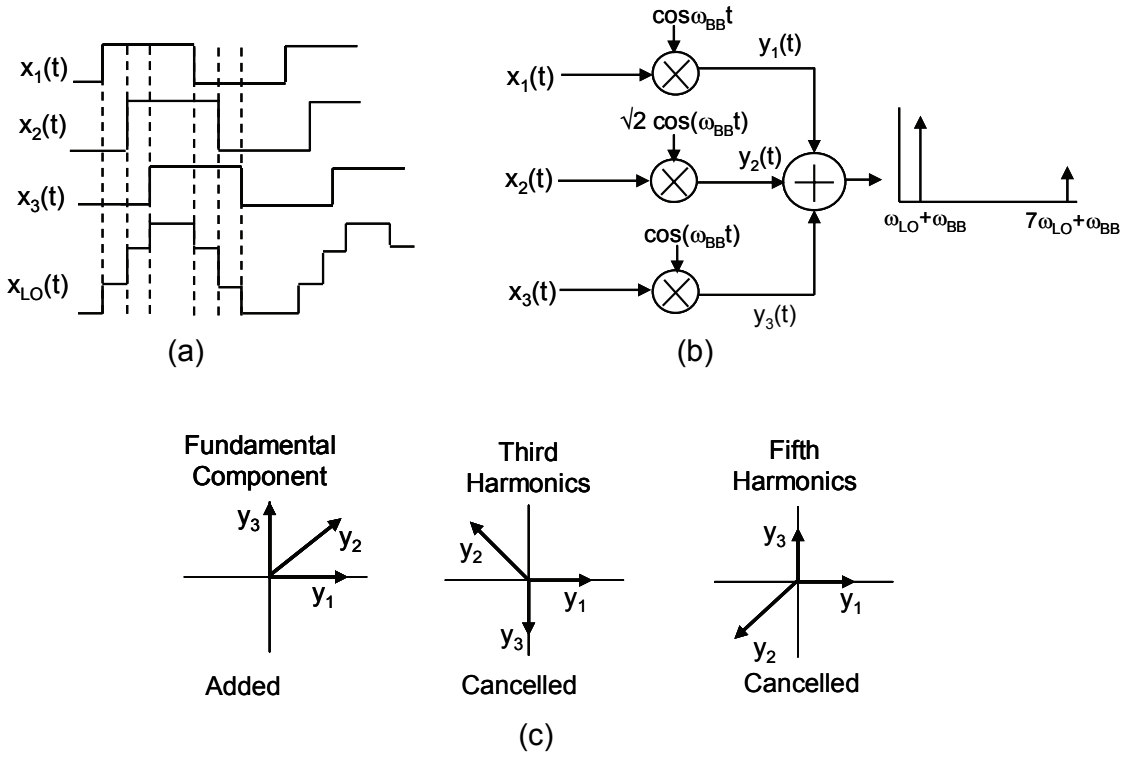


Figure 3.5: (a) Harmonic rejection signal generation, (b) HRM structure, (c) Vector addition of fundamental component, third harmonic and fifth harmonic

Comparison with the existing method for Harmonic Rejection

With the existing harmonic rejection technique only 3rd and 5th harmonics can be cancelled. So, the first non-cancelled harmonic is the 7th harmonic. But using the multi-path technique any higher order harmonics can be cancelled depending on the number of paths. To cancel higher harmonics (than 5th) by adding more paths in HRM technique seems not possible. Moreover, the non-linearity of the mixer can also generate strong even order harmonics which can not be cancelled with this HRM technique. But these can be cancelled with the multi-path technique. Similarly in HRM, the fundamental component in all paths are not exactly in the same phase. So they are only added up partially. But with the multi-path technique, they are always in the same phase at the output

3.2 Mixer as a phase shifter and frequency shifter

This section will discuss the realization of the phase shifters, the main building blocks in the polyphase multi-path system. Polyphase filter circuits for image filtering are often implemented using linear R-C networks or L-C networks to realize the required phase shift. Although these circuits are sometimes referred to as wideband, the fractional bandwidth of such circuits seldomly exceeds 50% [10], [11]. To realize wideband harmonic rejection using a polyphase multipath technique, we need circuits with a constant phase shift over a much wider range. This is because all phase shifters need to

have a constant phase shift over all relevant frequencies involved in the cancellation process. In a DSP intensive radio transmitter, digital signal processing techniques can be exploited to realize phase shifters before D/A conversion and nonlinear power amplification. Therefore, a good solution can be to shift this phase generation problem to the digital domain, and use a DSP followed by multiple DACs to generate multi-phase baseband signals. However, after the baseband we are in the analog domain. There can be many harmonics after the nonlinear element. In that case, cancellation of a multitude of harmonics requires a constant phase shift over many octaves of frequency.

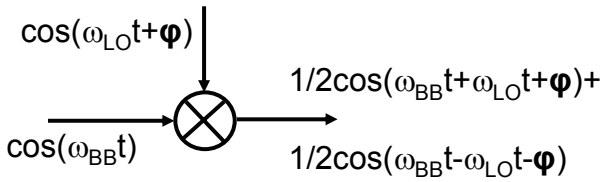


Figure 3.6: Mixer used as a wideband phase shifter

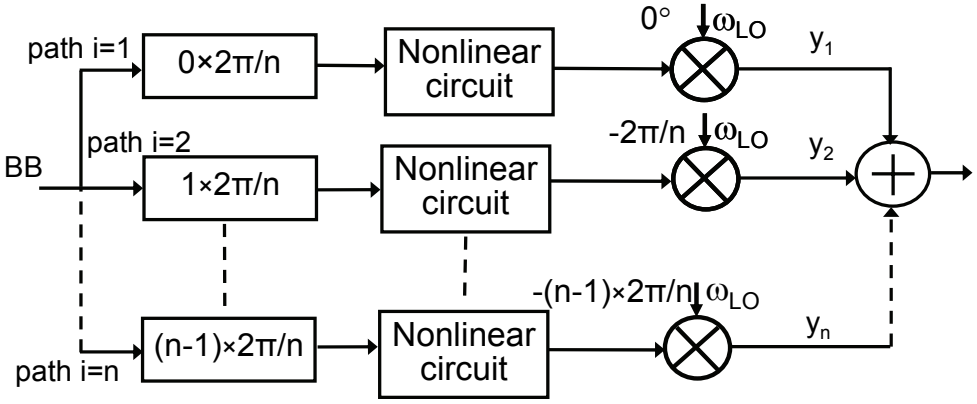


Figure 3.7: Phase shifter after the nonlinear circuit is replaced by a mixer

A very wideband phase shifter can be implemented with a mixer, since a mixer conveys phase information of both the "baseband" (BB) and "Local Oscillator" (LO) port to the output ("RF") port as shown in Figure 3.6. Whatever phase is added to the LO signal, it will appear at the output of the mixer[1]. So, by replacing the second set of phase shifters with mixers plus phase shift on the LO path (Figure 3.7), we can achieve a wideband phase shift but simultaneously we will have upconversion. As upconversion is desired in a wireless transmitter circuit anyway, this fits very nicely to our goal. The first set of phase shifters can be implemented in the digital domain as explained above. The effect of mismatch in phases is discussed in section 3.4.4.

An image component generated during the mixing is also cancelled by the polyphase multipath. This is discussed below.

[1] This also holds for higher harmonics of the LO signal and baseband input-signal, as long as speed limitations in the mixer play no significant role.

Single-Sideband Generation

When two signals with frequency ω1 and ω2 are multiplied, both a sum frequency and a difference frequency are obtained at the output as shown in equation 3.10. Usually only one of these is the wanted signal, while the other (undesired frequency) needs to be suppressed.

$$(A\cos\omega_1 t)\times(B\cos\omega_2 t)=\frac{AB}{2}\left[\cos(\omega_1+\omega_2)t+\cos(\omega_1-\omega_2)t\right] \qquad 3.10$$

The designer must provide a way to remove this undesired component. Figure 3.8(a) shows a well-known Weaver archetecture [12] to get the single sideband. The idea is to mix the signals both in quadrature (90^o out of phase) and in phase and then combine them such that one sideband is augmented and the other sideband is cancelled.

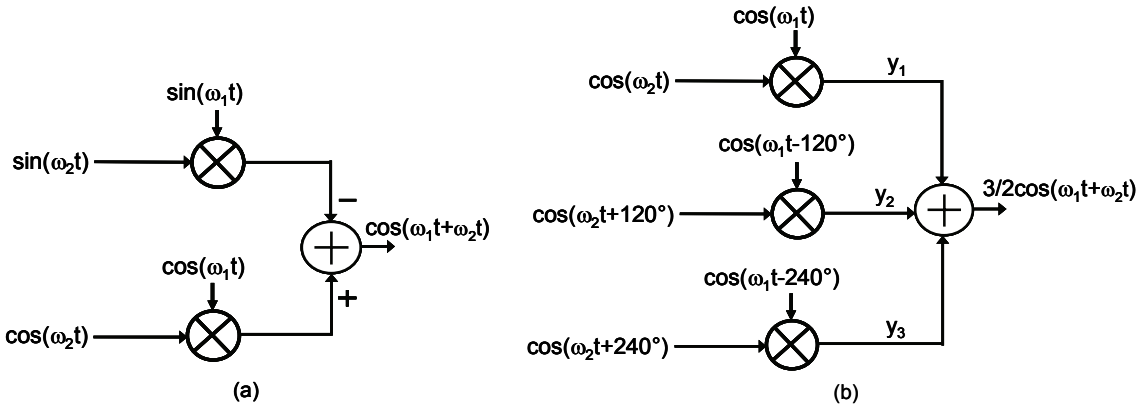


Figure 3.8: (a) conventional SSB mixing (b) mixing with polyphase multipath

A multi-path system as described in section 2.2 always cancels the image components. A three-path system shown in Figure 3.8(b) illustrates the single sideband property of a multipath system. The signals with the positive phase sequence 0°, 120° and 240° i.e. iφ are respectively multiplied with the negative phase sequence 0°, -120° and -240° i.e. -iφ. The resulting signal in each path will be:

$$y_0=\frac{1}{2}[\cos(\omega_2 t+\omega_1 t)+\cos(\omega_2 t-\omega_1 t)] \qquad 3.11$$

$$y_1=\frac{1}{2}[\cos(\omega_2 t+\omega_1 t)+\cos(\omega_2 t-\omega_1 t+240^\circ)] \qquad 3.12$$

$$y_2 = \frac{1}{2}[\cos(\omega_2 t + \omega_1 t) + \cos(\omega_2 t - \omega_1 t + 480^\circ)] \quad 3.13$$

The outputs of all three paths are then added.

$$y = y_0 + y_1 + y_2 = 3/2\cos(\omega_2 t + \omega_1 t) \quad 3.14$$

The image signals at the output y_0, y_1 and y_2 always add destructively. However, the up-converted signals are at the same phase so they are added up. In conclusion, the frequency translation in a multi-path system is single sideband.

Due to the non-linearity, the input signal to mixers in Figure 3.7 also contains the harmonics of the baseband input signal. Moreover, flexible frequency synthesizers rely on digital dividers and generally produce square-wave signals, while for power efficiency reasons it is highly desired to use a switching mixer and a large BB-signal swing. Therefore the output spectrum will now contain a forest of harmonics and sidebands at frequencies $k_{LO}\omega_{LO} \pm m\omega_{BB}$, where k_{LO} and m are integers, due to the multiplication of the square wave LO with the baseband input signal BB, and the nonlinearity of the circuit. In the next section we will see how we can exploit the polyphase multipath technique to cancel almost all the unwanted components.

3.3 Filter-less Power Upconverter Design

3.3.1 Basic Power Upconverter

A power up-converter (PU) combines the functionality of a power amplifier and upconversion mixer. The power amplifier and mixer can be as simple as shown in Figure 3.9, which is equivalent to first amplification and then mixing. Here the PA is a single transistor operating as transconductor (V-I converter), which is switched on and off by the LO signal via a switch. Thus the V-I conversion and upconversion is done in the same circuit, via a switched transconductor mixer [8]. With respect to efficiency this circuit resembles a single transistor (class A) power amplifier. However, due to the polyphase multipath technique distortion products are cancelled and larger signal swings can be tolerated, improving efficiency. A disadvantage of the PU is the power dissipation in practical switches (transistors). On the other hand, a narrowband filter behind a traditional power amplifier would also cause considerable power loss.

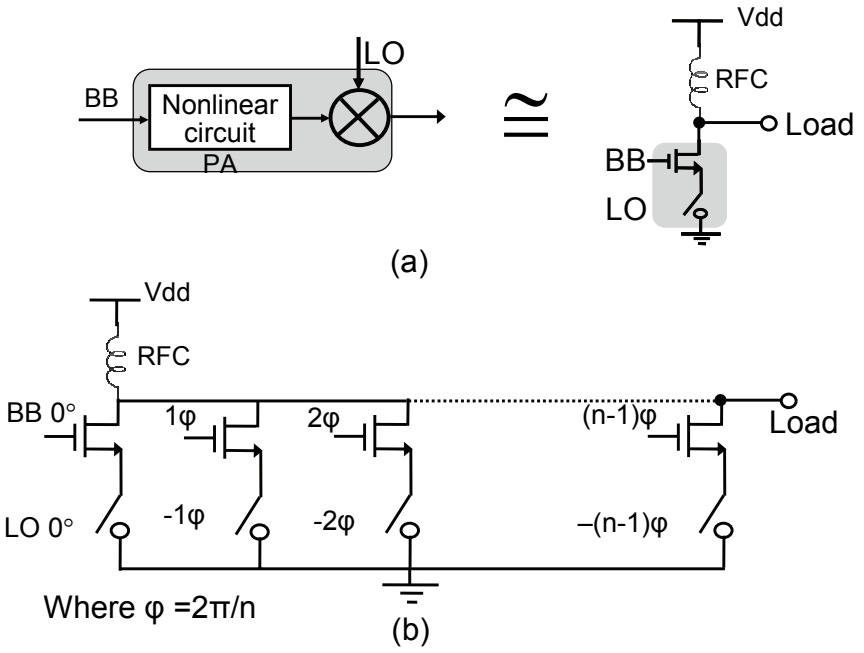


Figure 3.9: (a) Basic Power Upconverter (b) n-path power upconverter

3.3.2 n-path Power Upconverter

To get an idea of spectral products generated with the power upconverter circuit, the basic (Figure 3.9(a)) and the multipath power upconverter were simulated in Matlab. Nonlinear circuits were modeled by a power series expansion, while ideal phase shifters were used. Figure 3.10 shows the spectral components (at $k_{LO}\omega_{LO} \pm m\omega_{BB}$) generated by a single-path PU for a single tone BB signal, i.e. the case where the polyphase multipath technique is not used. Clearly, nonlinearities and switching behavior result in a forest of strong harmonics and sidebands. To clean up the spectrum by using the multipath technique, we divide the PU into 'n' identical smaller pieces, driven by BB and LO signals having equal but opposite phases, and then simply add their output currents at the output node as shown in Figure 3.9(b). The phase shift at the baseband input is 0, 1φ, 2φ….(n-1)φ and its opposite phase is applied via the LO signals.

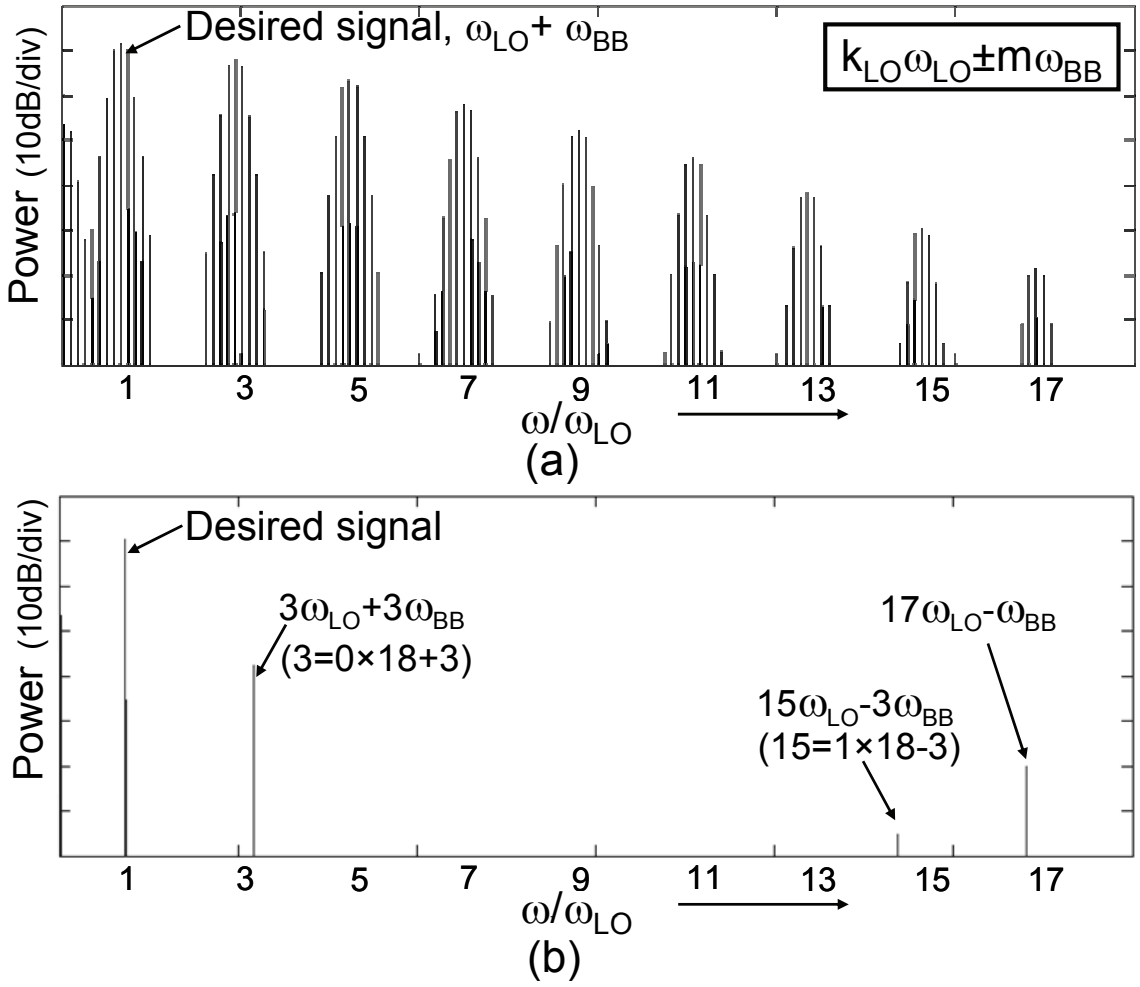


Figure 3.10: Output spectrum (a) Basic power upconverter (b) 18-path power Upconverter

Figure 3.10(b) shows the output of a polyphase 18-path circuit (see section 3.4 for a motivation for the choice of the number of paths): most of the harmonics and sidebands are cancelled now. Unfortunately, a few are still present at the output. Since we have two input ports now (BB and LO), and mixing produces a sum and difference frequency, a slightly different condition for non-cancelled products is found [5]:

$$k_{LO}=j\times n+m \qquad \text{where } j=\ldots.-2, -1, 0, 1, 2\ldots. \qquad 3.15$$

and m is a positive or negative integer number. The most important non-cancelled products are at $3\omega_{LO}+3\omega_{BB}$, $5\omega_{LO}+5\omega_{BB}$, $7\omega_{LO}+7\omega_{BB}$ (j=0) and $15\omega_{LO}-3\omega_{BB}$, $13\omega_{LO}-5\omega_{BB}$ (j=1). The product of the magnitudes of the respective harmonics of ω_{LO} and ω_{BB} determines the strength of these products. For a unity magnitude LO squarewave, harmonic k_{LO} is k_{LO} times smaller then the fundamental. If we assume that the nonlinear circuit operates at its 1-dB compression point (to obtain high output power and efficiency)

for an input signal Acos(ω_{BB}t), and a_1, a_5, a_7 are the coefficients of the nonlinearity, the magnitude of the $5\omega_{LO}+5\omega_{BB}$, $7\omega_{LO}+7\omega_{BB}$ products are $\left(\frac{A^4 a_5}{5\times 16 a_1}\right)$, $\left(\frac{A^6 a_7}{7\times 64 a_1}\right)$ respectively lower than the magnitude of the wanted signal at ($\omega_{LO}+\omega_{BB}$). These higher order terms are much smaller than the wanted signal, similar conclusions hold for the j=1 products. As a result these products are typically smaller than residual products caused by inaccuracies like device and phase mismatch and it does not make much sense to cancel them. Still, the $3\omega_{LO}+3\omega_{BB}$ is troublesome because the 3rd order distortion term is usually much stronger than higher order distortion components [9] and is also close to the desired signal. It cannot be cancelled with any number of paths because in equation 3.15 j=0 for this case, so independent of n.

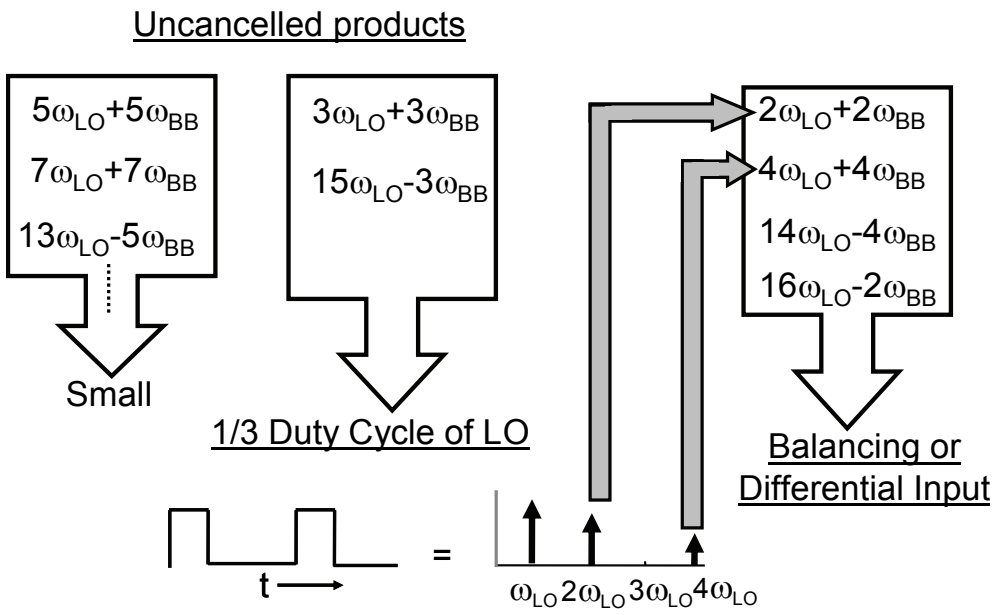


Figure 3.11: Overview of solutions for the non-cancelled product: the use of a square wave LO with 1/3 duty cycle

1/3 Duty Cycle Technique

To eliminate the strong $3\omega_{LO}+3\omega_{BB}$ terms, the duty cycle of the LO was chosen to be 1/3. From the Fourier series expansion, the amplitude of the fundamental and harmonics of a square-wave as a function of the duty cycle 'd' is given by

$$V_n = \frac{A}{k_{LO}\pi}\sqrt{2-2\cos(2\pi k_{LO} d)} \qquad 3.16$$

where A is the amplitude of the square-wave and k_{LO} is the order of the harmonics.

So from equation 3.16 when the duty cycle is 1/3, the 3rd, 6th, 9th, 12th, 15th etc harmonic term disappears from the Fourier series expansion. Thus the troublesome terms at $3\omega_{LO}+3\omega_{BB}$ and $15\omega_{LO}-3\omega_{BB}$ are also rejected, while other terms are small enough. However, a 1/3 duty cycle also means that there will be harmonics with even coefficients like $2\omega_{LO}$, $4\omega_{LO}$ etc. So other distortion products like $2\omega_{LO}+2\omega_{BB}$, $4\omega_{LO}+4\omega_{BB}$, $14\omega_{LO}-4\omega_{BB}$, $16\omega_{LO}-2\omega_{BB}$ appear instead. Fortunately, it is quite easy to cancel these products by using a differential baseband input (balancing). This is desired anyhow for rejecting common mode interference like substrate and supply bounce. Figure 3.11 and Table 3.1 give an overview of how different unwanted products are cancelled with the various techniques. 'M' indicates cancellation by the multi-path technique, 'D' by 1/3 duty cycle of the LO and 'B' by balancing. Multiple letters in the table mean that the harmonic is cancelled by more than one technique. The first significant non-cancelled product for an 18-path system with 1/3 duty cycle and balanced BB-signals is $17\omega_{LO}-\omega_{BB}$.

m ⟶	-4	-3	-2	-1	0	1	2	3	4
$1\omega_{LO}+m\omega_{BB}$	BM	M	BM	M	M		BM	M	BM
$2\omega_{LO}+m\omega_{BB}$	BM	M	BM	M	M	M	B	M	BM
$3\omega_{LO}+m\omega_{BB}$	BMD	MD	BMD	MD	M	MD	BMD	D	BMD
$4\omega_{LO}+m\omega_{BB}$	BM	M	B	M	M	M	BM	M	B
$5\omega_{LO}+m\omega_{BB}$	BM	M	BM	M	M	M	BM	M	BM
$6\omega_{LO}+m\omega_{BB}$	BMD	MD	BMD	MD	M	MD	BMD	MD	BMD
$7\omega_{LO}+m\omega_{BB}$	BM	M	BM	M	M	M	BM	M	BM
$8\omega_{LO}+m\omega_{BB}$	BM	M	BM	M	M	M	BM	M	BM
$9\omega_{LO}+m\omega_{BB}$	BMD	MD	BMD	MD	M	MD	BMD	MD	BMD
$10\omega_{LO}+m\omega_{BB}$	BM	M	BM	M	M	M	BM	M	BM
$11\omega_{LO}+m\omega_{BB}$	BM	M	BM	M	M	M	BM	M	BM
$12\omega_{LO}+m\omega_{BB}$	BMD	MD	BMD	MD	M	MD	BMD	MD	BMD
$13\omega_{LO}+m\omega_{BB}$	BM	M	BM	M	M	M	BM	M	BM
$14\omega_{LO}+m\omega_{BB}$	B	M	BM	M	M	M	BM	M	BM
$15\omega_{LO}+m\omega_{BB}$	BMD	D	BMD	MD	M	MD	BMD	MD	BMD
$16\omega_{LO}+m\omega_{BB}$	BM	M	B	M	M	M	BM	M	BM
$17\omega_{LO}+m\omega_{BB}$	BM	M	BM		M	M	BM	M	BM

M=cancelled by multi-path, D=cancelled by 33% duty cycle, B=cancelled by balancing

Table 3.1: The cancellation of unwanted products in a 18-path pu with different techniques: m=cancelled by multi-path; d=cancelled by 33% duty cycle, b= cancelled by balancing (differential)

3.4 Circuit Implementation

3.4.1 Overview

To demonstrate the feasibility of a highly flexible multipath upconverter, we designed a PU in a 0.13µm CMOS process, covering all radio bands between DC and 2.4GHz. Assuming a signal swing in the order of the standard supply voltage of 1.2V, it is possible to deliver about 10mW power directly to a differential 100Ω load, which is sufficient for many short range communication links. The differential load is converter to single ended (50Ω) via the off-chip transformer. If more output power is needed, the impedance matching ratio i.e. the turns ratio of the transformer can be increased. To maximize the experimental flexibility and frequency range, we implemented the LO phase generation "brute force" via a shift register running at 9 times the LO frequency in our test chip. This enabled us to evaluate the circuit for an arbitrary LO frequency between DC and a maximum given by the speed limitation of the logic used to realize the shift register. A DLL could be used to achieve even higher LO-frequencies, provided it has enough phase accuracy. However, it is shown in [13] that a shift register based multiphase clock generation circuit almost always generates less jitter than a DLL equivalent at a given power budget because the former has no jitter accumulation from one clock phase to the other. Other frequency synthesis techniques might be more appropriate and use less power. However, the key aim of this chip was to demonstrate the feasibility and RF-performance of a polyphase multipath PU-core. For experimental freedom, also the baseband polyphase signal generation was done off-chip.

The number of paths 'n' was chosen because of the following reasons. To generate square wave signals with 1/3 duty cycle and with the desired phase shifts from a high-speed clock, multiples of 3 are best suited for n. Furthermore to utilize both the positive and negative edge of the clock, an even number of paths is desired so that the clock frequency needed will only be a factor of n/2 higher than the output frequency. The resulting suitable values of n are 6, 12, 18 etc and we have chosen 18 paths in our test chip to demonstrate that the technique can cancel a large multitude of harmonics and sidebands. To show that it can also work up for LO frequencies in the gigahertz region, we added the option to use 6 paths as well and designed the logic to run at 7.2GHz resulting in 2.4GHz maximum LO frequency (and maximally 800MHz in 18-path mode).

3.4.2 Multiphase Signal Generation Circuit

For 18 paths we need LO signals of 18 different phases (0°, 20°, 40° …340°). Moreover, the square wave should have 1/3 duty cycle. Applying a positive and a negative clock edge alternately to successive latches in a chain of 18 D-latches (see Figure 3.12(a)), 18 different phases are produced (see Figure 3.12). However, the duty cycle at the output is 1/2. The feedback through the NOR gate is used to make the duty cycle 1/3.

In Figure 3.12(a), if the initial state of all the latches is assumed zero, then the input to the first latch will be '1'. In each rising or falling edge, this '1' will travel to the consecutive D-latches (from left to right). When the output Q5 becomes '1', the input to the first latch

becomes ‘0’. Now this ‘0’ starts to travel to the consecutive D-latches with each rising or falling edge of the clock. But when the state of the D-latch at Q5 and Q11 is ‘0’, the input to the first latch is again ‘1’. So the cycle repeats after each nine clock cycles. Except in the first cycle, the contents of 6 latches are ‘1’ and the remaining (12) latches are ‘0’ creating a 33% duty cycle at the output of each D-latch.

To minimize the phase mismatch, the load of all the latches is made equal by adding dummy loads appropriately. Two sets of buffers are used in between the latches and the PU; one to drive the long wires between them and another to drive the switches of the PU. Note that the long wires are needed due to the bond-pad limitation of the chip (see Figure 3.14).

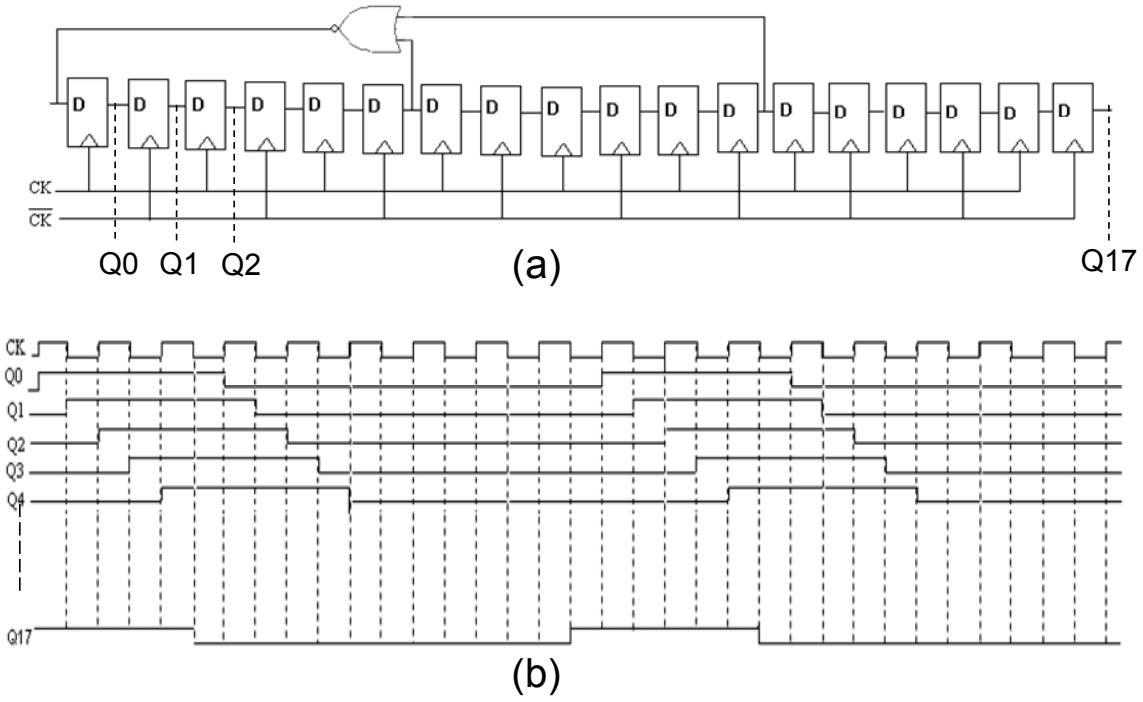


Figure 3.12: (a) LO phase generation circuit (b) Output: 18 phase LO signals

To minimize cross-talk generation of the digital components of the divider chain to the PU, the latches, gates and buffers are designed using current mode logic (CML). The buffers that drive the PU- switches have an output swing of approximately 850mV (0.35-1.2V), sufficient to switch the PU. The latches, NOR gate and remaining buffers all have an input/output swing of approximately 600mV (0.6-1.2V). Dimensioning of the CML circuits, especially the latches, was done to maximize the speed. Increasing the tail current and the size of these CML cells simultaneously will result in an increase in speed as long as the load capacitance dominates the cell’s own output capacitance [14].

In our experimental setup, the 9 differential baseband voltages with different phases are generated off-chip. The signals were generated via a vector modulator, by weighted addition of a sine and cosine wave. Since the baseband signals are at much lower frequency compared to the LO, it is easier to realize sufficient phase accuracy (see next

section) and no tuning was required on our baseband signal generation board. More work has to be done to explore the most effective way to generate multi phase baseband signals on-chip via DSP techniques and multiple DACs.

3.4.3 Power Upconverter Circuit

Figure 3.13 shows the 18-path power upconverter. Each path consists of a switched transconductor mixer with a baseband signal applied to a differential pair, acting as the transconductor, and an LO signal driving a grounded switch. The wanted output signals from all paths add up in phase, so the total area and power of the power upconverter core is not increased by splitting it into 18 paths. Since all the paths are identical, the design of the PU is quite straightforward. The complete PU is biased at the supply voltage through RF chokes to increase the output swing and efficiency, as commonly done in power amplifier design. The inductance of the chokes puts a lower limit to the RF frequency, but the chip can work at arbitrarily low frequency. Operating each individual mixer at the 1dB compression point, the PU is designed for a large output swing of $2.54V_{\_pp\_diff}$ over the load (e.g., antenna) to get a good efficiency. This is close to the maximum swing that can be achieved from 1.2V supply while keeping the upper transistor (transconductance transistor) of the PU in saturation. To further increase the output power without adding an external power amplifier, a transformer could be added for broadband impedance transformation.

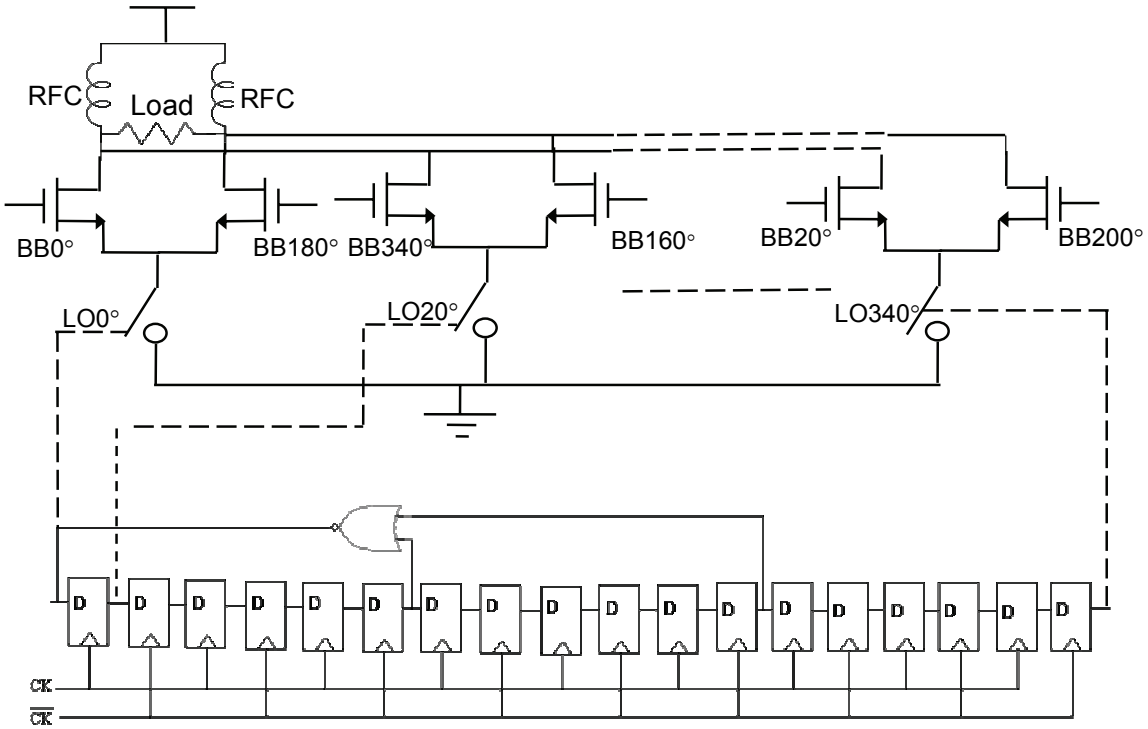


Figure 3.13: Power Upconverter using polyphase 18-path architecture

Wide switch transistors are beneficial to reduce the static power dissipation in the switches but require more power in the driver buffers. This trade-off is one factor that determines the size of switch. On the other hand it is beneficial to choose the size of the transconductance and switch transistors roughly equal to maximize the amplification for minimal total width (area). The W/L ratio that was chosen for each transconductance- and switch transistor is 64/0.13 and 50/0.13 respectively. The resulting voltage conversion gain of the PU with the 1/3 duty cycle of the LO will be approximately $\sqrt{3}G_m R_L / \pi$, where G_m is the overall transconductance of the PU. Biasing is another important issue in a PU design. The bias voltage was chosen as low as possible, but still high enough to to keep the transconductance transistor in strong inversion and saturation for the full cycle of the input voltage (if the switch is ON). This helps to minimize the dc current and hence improve efficiency.

3.4.4 Mismatch

In practice, perfect cancellation of harmonics and sidebands is not possible due to the presence of mismatch between the paths. The effect of gain and phase mismatch on the cancellation of harmonics will be discussed in this section. If θ, and δ are the phase mismatch in the baseband and LO signals respectively and ε is the gain mismatch between the paths, then the suppression the $k_{LO}\omega_{LO} \pm m\omega_{BB}$ harmonic in the presence of mismatch is given by [5]:

$$E(HRR_{k,m}) = \frac{P_{k,m,reference}}{P_{k,m,rejected}} = \frac{N^2}{(N-1)\left(\frac{\sigma_\varepsilon^2}{a_1^2} + k_{LO}^2\sigma_\theta^2 + m^2\sigma_\delta^2\right)} \qquad 3.17$$

where $\sigma_\theta^2, \sigma_\delta^2$ and σ_ε^2 are the variances of the stochastic variables θ, δ and ε respectively and E() is the expectation operator. N is the number of paths. This equation predicts that the effect of phase mismatch is higher for higher harmonics because of k^2_{LO} and m^2 terms. However higher order harmonics are relatively weak. Interestingly, a higher number of paths is beneficial to suppress the harmonics more effectively in the presence of mismatch. Equation 3.17 also shows that the effect of device mismatch is constant for all the harmonics. Since a power upconverter uses large devices to produce sufficient output power, the device mismatch term is typically less important than the phase mismatch.

To get a feeling of the suppression of harmonic in the presence of mismatch, we calculate the harmonic rejection ratio (HRR) for $2\omega_{LO}+\omega_{BB}$ as an example using equation 3.17. With σ_ε=0.03 (3 % gain mismatch) and $\sigma_\theta=\sigma_\delta$=0.017 (1° phase mismatch) and for gain, a_1=1, the expected HRR of $2\omega_{LO}+\omega_{BB}$ predicted by equation 3.17 is 39.1dB. It is worth mentioning that the harmonic $2\omega_{LO}+\omega_{BB}$ is 6dB lower than the desired signal, $\omega_{LO}+\omega_{BB}$, even without cancellation. So the harmonic $2\omega_{LO}+\omega_{BB}$ is expected to be at 45.1dB below the desired signal after cancellation with the above gain and phase mismatch parameter.

In our design, different design measures were taken to keep the phase of the different paths equal. For example loading of all the latches and buffers in the divider chain are made equal by adding dummy loads and, the path length from dividers to PU for all paths was kept equal. A thorough mathematical analysis of the mismatch can be found in [5].

3.5 Experimental Results

A demonstrator chip of the proposed polyphase multipath power upconverter was designed and fabricated in a 0.13-µm CMOS process. The chip has a standard supply voltage of 1.2V and has an option to select a 6- and 18-path operation mode. The die micrograph is shown in Figure 3.14. The chip is clearly bond pad limited for reasons of experimental flexibility. The active area of the two rectangular blocks, PU and dividers and buffers, shown in the Figure 3.14, is only 0.14mm^2. Between them are just wires to connect them. The baseband bandwidth is 1Hz to 50 MHz. During evaluation, the input baseband signal was arbitrarily chosen at 100 kHz, while varying the LO frequency between 0 and 2.4 GHz. No filters are used at the output. The RF choke (RFC in Figure 3.13) and load are off chip. Operating each individual mixer at the 1dB compression point, the PU delivers 8mW power to the 100Ω load.

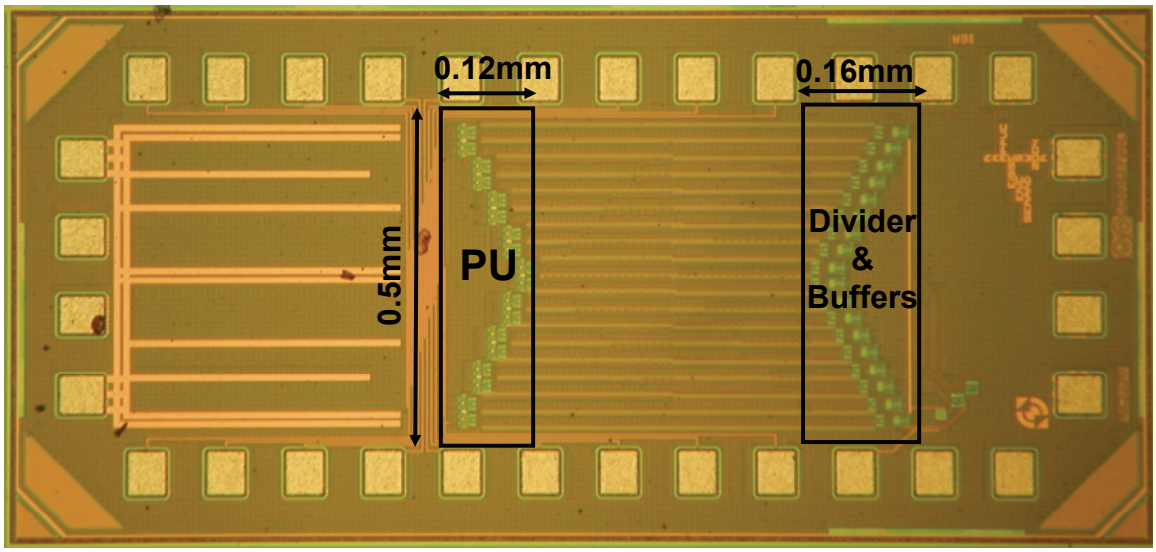


Figure 3.14: Demonstrator Chip Micrograph

Figure 3.15(a) shows the measured output spectrum of a single-path power upconverter, which means without using the polyphase multipath technique. The frequency of the LO is 350MHz. Please note that the unfortunate FM radio broadcast spurs that are modulated with our output signal, are due to a 100.0MHz, 10kW FM radio broadcast transmitter on the roof of our building. The suppression of the 3rd, 6th, etc harmonics is due to the 1/3 duty cycle of the LO. Because of the large frequency-scale, the sidebands around the fundamental and harmonic are not visible in this figure. Figure 3.15(b) shows the measured spectrum after the cancellation by a polyphase 18-path circuit. All the harmonic products are effectively suppressed to -48dBc.

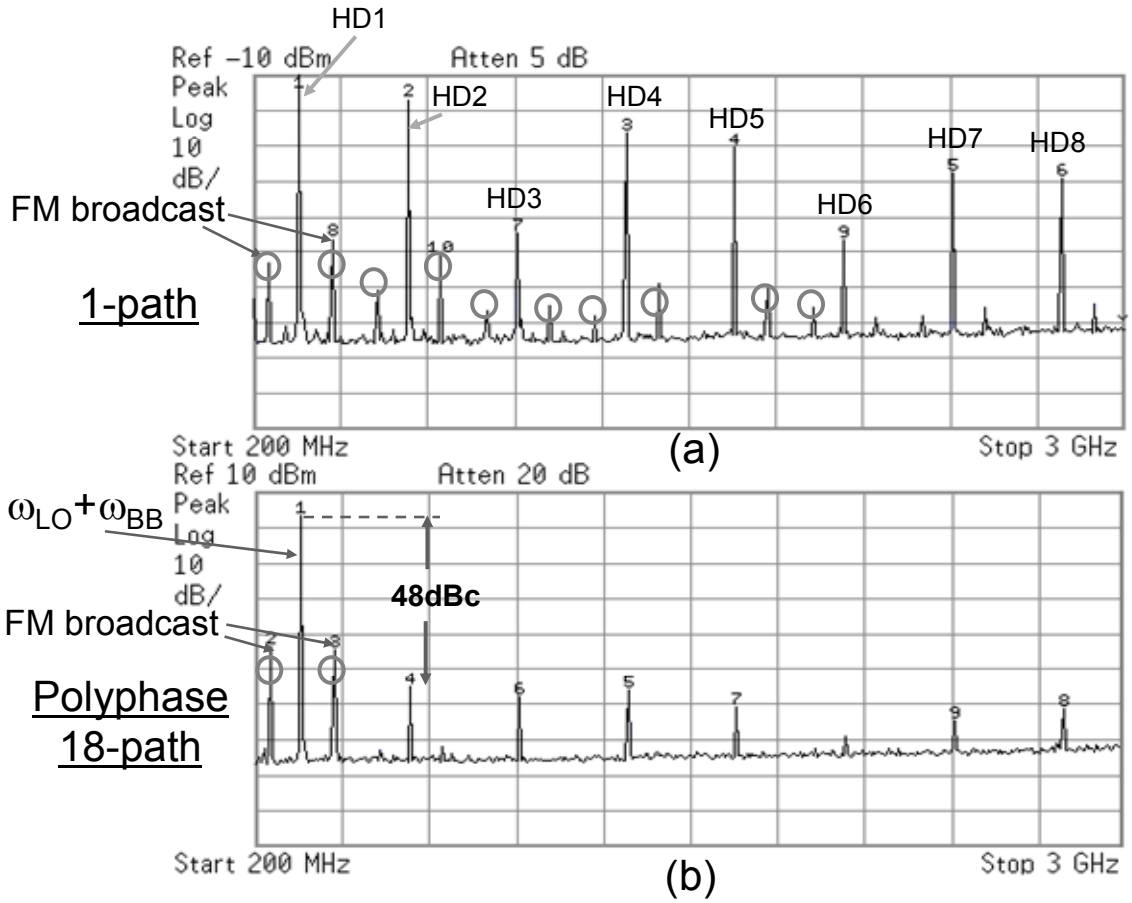


Figure 3.15: Output spectrum (a) before cancellation (b) after cancellation

Figure 3.16(a) shows the measured upconverted signal (desired signal), its image and LO feed-through (carrier) with only one path. The suppression of the image and the LO feed-through due to the polyphase 18-path circuit is shown in Figure 3.16(b). All the sideband products are suppressed to 39dB below the desired signal.

In order to demonstrate the wideband cancellation property, we used a relatively low frequency LO of 80MHz. Now all harmonics up to 2GHz are visible without attenuation in Figure 3.17. It shows the first non-cancelled harmonic $17\omega_{LO}$-ω_{BB} at 1.3599 GHz as predicted by the theory. The output spectrum is cleaned up to the 17th harmonic of the LO, with a worst case spur at -46dBc. Figure 3.18 shows the spectrum for a high output frequency of 2.1GHz with a 6-path circuit. It shows a first non-cancelled harmonic $5\omega_{LO}$-ω_{BB} (10.4999GHz) as predicted by the theory and a worst case spur at -46dBc up to this frequency.

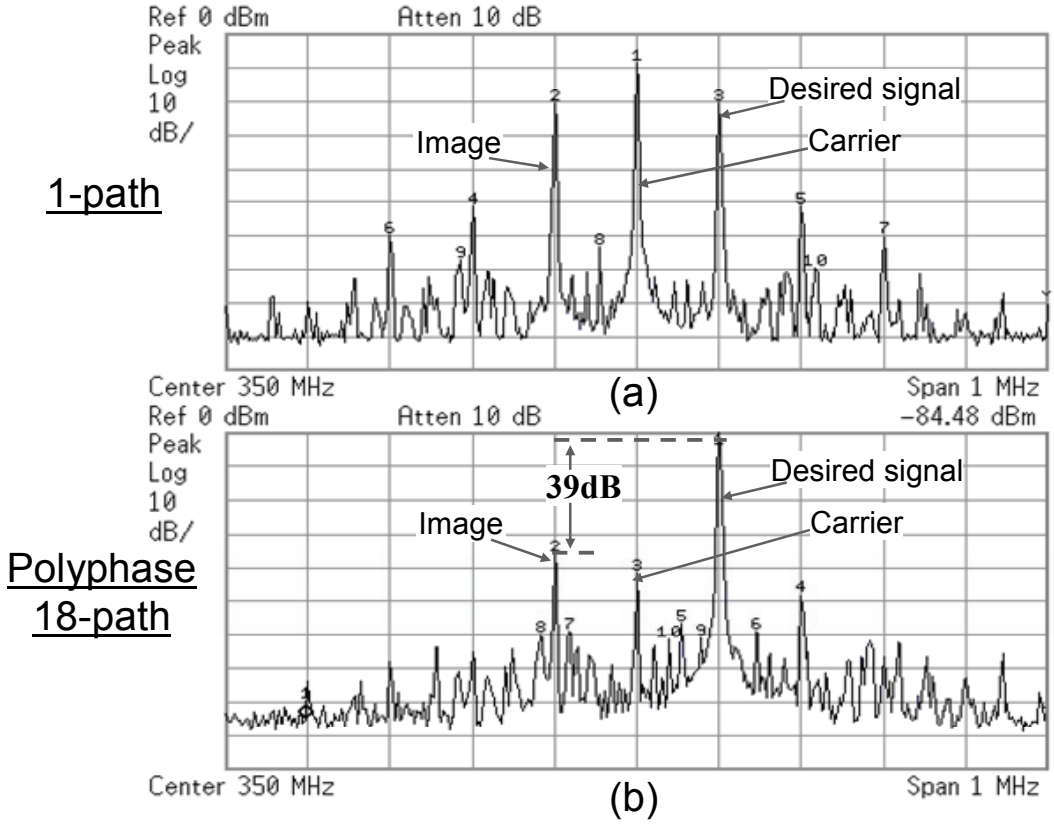


Figure 3.16: The LO leakage and image rejection performance (a) before cancellation (b) after cancellation

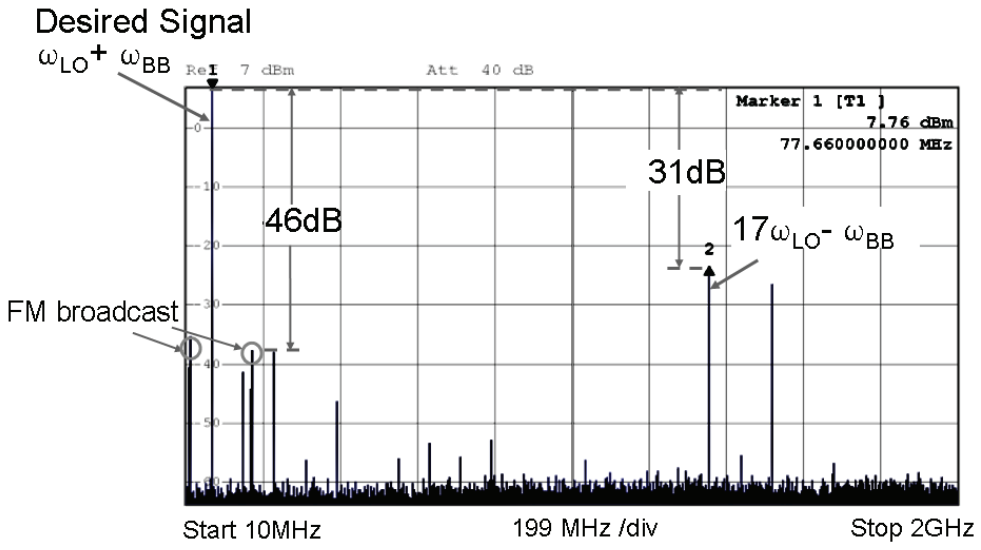


Figure 3.17: Output spectrum for 80MHz carrier

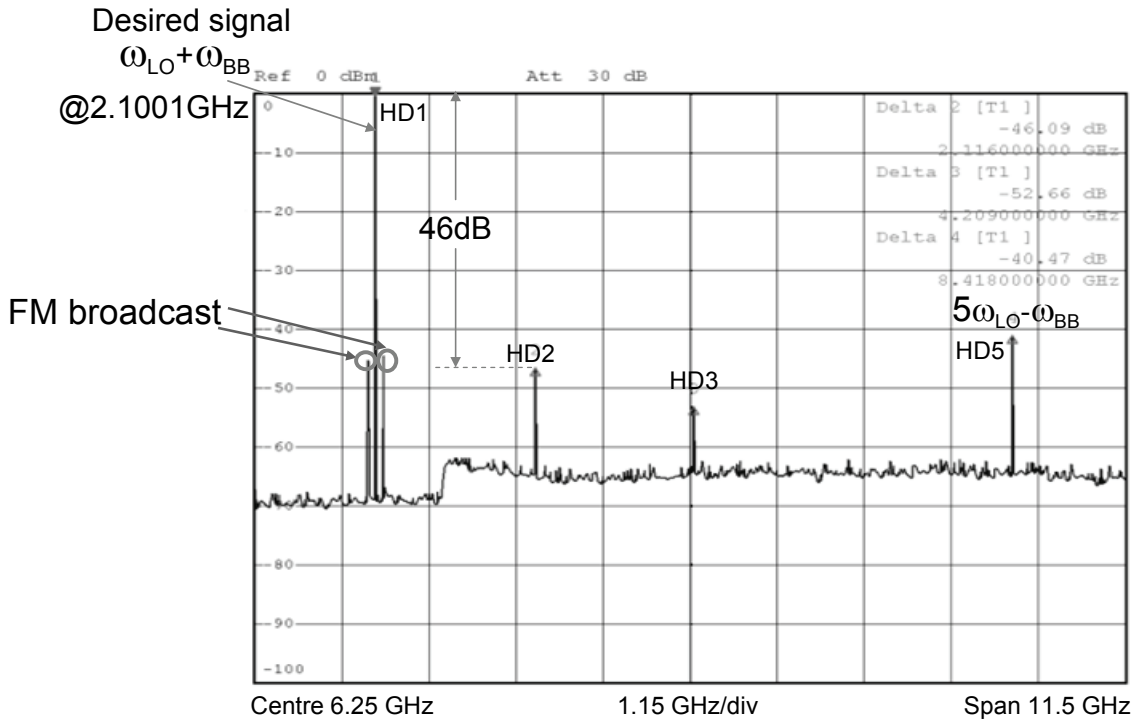


Figure 3.18: output spectrum with 6-path for 2.1GHz carrier

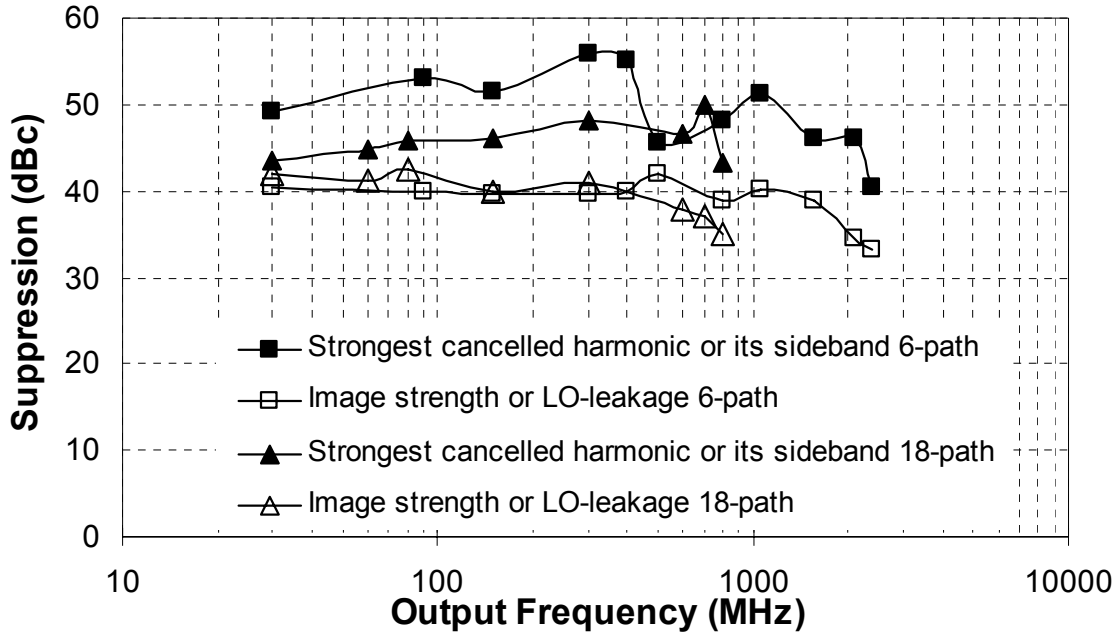


Figure 3.19: Measured suppression of undesired products over the full output frequency range

Figure 3.19 shows results of the harmonic rejection over the entire 2.4GHz band of LO-frequencies, and also for image rejection and LO-leakage. The LO frequency is varied from 30 MHz to 800MHz for the 18-path PU and the strongest cancelled harmonics or sidebands are measured and plotted. For the 6-path PU this was also done, but now by varying the LO frequency from 30 MHz to 2.4 GHz. This figure shows that the worst case harmonic spur is smaller than -40 dBc in the entire frequency range. As the LO frequency reaches its limit, the spurs increase most probably due to an increase in phase mismatch. But still the harmonic spurs remain below -40dBc. The maximum clock frequency at which the circuit works is 7.2GHz. The maximum LO frequency is thus 2.4 GHz for 6-path mode and 800 MHz for 18-path mode, as the clock frequency is divided 3 and 9 times respectively. We did not test the PU using any particular standard. However in simulation we did test the PU with a two-tone signal and also a detailed mathematical analysis of it can be found in [5].

We also measured 20 samples of the IC at 350MHz carrier frequency. All the harmonic spurs were smaller than -46dBc for all the samples. $2\omega_{LO}+\omega_{BB}$ and $2\omega_{LO}-\omega_{BB}$ are the dominant harmonic spurs as these products are close to the fundamental and hence the strongest (just 6dB below the carrier before cancellation). So the harmonic rejection for those products is better than 40dB for 20 samples with a polyphase 18-path PU. From mismatch equation 3.17, this corresponds to 1.3° of phase mismatch in the LO path, neglecting the phase mismatch in the BB signals (since they are at low frequency) and the device mismatch (since large devices are used in the PU).

We tried to measure the output noise of the PU, but it was lower than the spectrum analyzer (ROHDE & SCHWARZ FSP 40GHz) noise floor for the required dynamic range. Simulation result predict a thermal output noise voltage of -166dBV/√Hz in 100ohm (assuming the phase noise of the LO is negligible) and a 1/f corner frequency of 10MHz from the LO. The G_m of the PU is 28mS, rendering about 6dB Noise Figure for the power upconverter. It is worth noting that the switched transconductor mixer has better thermal noise performance compared to a Gilbert mixer [8].

Technology		0.13μm CMOS
Supply Voltage		1.2V
Output Power		8mW
Output Swing		$2.54V_{pp\text{-}diff}$
Load		100Ω (diff)
Power Consumption	Digital circuits	156mW
	PU core	72mW
	Total	228mW
Worst case Harmonic Rejection (20 samples)		-40dBc

Table 3.2: Other performance

The performance parameters of the PU are summarized in Table 3.2. The PU delivers 8mW of output power to a 100Ω load with a drain efficiency of 11%. The output swing is 2.54Vpp-diff. The total power consumption is 228mW. The power consumption of the digital circuits; divider and buffers is currently high i.e. 156mW. One reason for this is the power consumption in driving the long wires between PU and LO generation circuits. In retrospect it would have been better to keep this much shorter, which would save one set of drivers (34 mW). Another reason is the use of current mode logic circuits for multiphase signal generation that are pushed for high operating frequency with high bias currents. By using standard logic gates or other smarter clock generation architectures we believe that the power consumption can be reduced significantly. Future CMOS processes with faster transistor will help to increase the frequency range in the current clock generator, and reduce its power consumption.

3.6 Conclusion

A key fundamental problem in radio circuits is their nonlinear and/or time-variant nature. As a result, they produce not only a wanted output signal, but also many unwanted harmonics and sidebands. This chapter present a power upconverter with a clean output spectrum up to the 17th harmonic of the LO (18-path mode) or 5-th harmonic of the LO (6-path mode) by using a polyphase multipath technique in combination with an LO with 1/3 duty cycle. Fabricated in a 0.13-µm CMOS process, it operates from DC to 2.4GHz with worst case harmonic rejection of 40dB over 20 samples. It uses no dedicated filters, but only digital blocks and switched transconductor mixers, making the design suitable for future Software Defined Radio architectures in CMOS. Further downscaling of CMOS processes is expected to relax the frequency range limitation in the current clock generator, and reduce its power consumption.

References:

[1] J. A. Weldon, J. Rudell, L. Lin, R. Narayanswami, M. Otsuka, S. Dedieu, L. Tee, K, Tsai, C. Lee, and P. Gray, “A 1.75-GHz highly integrated narrow-band CMOS transmitter with harmonic-rejection mixers”, *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 2003–2015, December 2001

[2] J. Kim, S. Kim, J. Shin, Y. Kim, J. Min, K. Kim, and H. Shin, “A CMOS Direct Conversion Transmitter with Integrated In-Band Harmonic Suppression for IEEE 802.22 Cognitive Radio Applications”, *IEEE Custom Intergrated Circuits Conference (CICC)*, pp. 603-606, September 2008

[3] P. Eloranta, and P. Seppinen, "Direct-Digital RF Modulator IC in 0.13µm CMOS for Wide-Band Multi-Radio Applications", *ISSCC Dig. Tech. Papers*, pp. 532-533, February 2005

[4] A. Flament, A. Frappe, A. Kaiser, B. Stefanelli, A. Cathelin, and H. Ezzeddine, “A 1.2 GHz semi-digital reconfigurable FIR bandpass filter with passive power combiner” *European Solid-State Circuits Conference (ESSCIRC)*, pp. 418-421, September 2008

[5] E. Mensink, E.A.M.Klumperink, and B.Nauta, “Distortion Cancellation by Polyphase Multipath Circuits”, *IEEE Transactions on Circuits and Systems-I*, pp. 1785-1794, September 2005

[6] R. Shrestha, E. Mensink, E.A.M Klumperink, G.J.M. Wienk, and B. Nauta, “A Multipath Technique for Canceling Harmonics and Sidebands in a Wideband Power Upconverter”, *ISSCC Dig. Tech. Papers*, pp. 452-453, February 2006

[7] R. Shrestha, E. Mensink, E.A.M. Klumperink, G.J.M. Wienk, and B. Nauta, "A Polyphase Multipath Technique for software-defined radio transmitters" *IEEE Journal of Solid State Circuits*, Vol. 41, pp. 2681-2692, December 2006

[8] E.A.M. Klumperink, S.M. Louwsma, G.J.M. Wienk, and B. Nauta, "A CMOS Switched Transconductor Mixer", *IEEE Journal of Solid-State Circuits*, Vol. 39, No. 8, pp. 1231-1240, August 2004

[9] W. Sansen, “Distortion in Elementary Transistors Circuits”, *IEEE Trasactions on circuits and systems*-II: *Analog and Digital Signal Processing*, Vol. 46, No. 3, March 1999

[10] F. Behbahani, Y. Kishigami, J. Leete, and A. Abidi, “CMOS Mixers and Polyphase Filters for Large Image Rejection”, *IEEE Journal of Solid-State Circuits*, Vol. 36, No. 6, pp. 873-887, June 2001

[11] M.J. Gingell, “Single sideband modulation using sequence asymmetric polyphase networks”, *Electrical communication, vol. 44*, pp. 1703-1705, 1973

[12] D. Weaver, “A third method of generation and detection of single-sideband signals,” *Proc. IRE*, vol. 44, no. 12, pp. 1703–1705, December 1956

[13] X. Gao, E.A.M. Klumperink, and B. Nauta, "Advantages of Shift Registers over DLLs for Flexible Low Jitter Multi-phase Clock Generation", *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 55, No. 3, pg. 244-248, March 2008

[14] R.C.H. van de Beek, “High speed Low-jitter frequency multiplication in CMOS”, Ph. D. dissertation, University of Twente, The Netherlands, 2004 (web-download: http://icd.el.utwente.nl/publications/)

Chapter 4

Polar Modulated Power Amplifiers

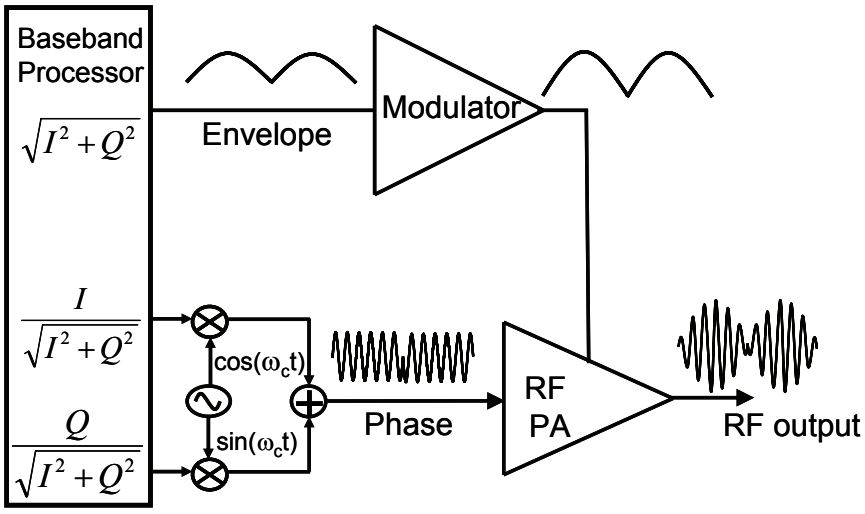


Figure 4.1 Polar modulated transmitter architecture

As discussed in previous chapters, amplifying a variable envelope signal with high peak to average power ratio using a conventional linear Power Amplifier (PA) suffers from poor efficiency because these PAs inherently operate far below their saturated output power level where the efficiency is maximum. Polar modulation transmitter architectures, where a phase modulated signal with constant envelope is amplified by a non-linear PA and the amplitude information is restored via its power supply modulation as shown in Figure 4.1, have the potential to enhance the efficiency while achieving sufficient linearity.

The supply modulator and the RF power amplifier are the two key building blocks of the polar modulated transmitter architecture shown in Figure 4.1. State-of-the-art implementations [1], [2], [3], [4] of supply modulators are reported either only for standards with at most a few MHz of signal bandwidth, due to strong requirements in the

supply modulator to satisfy the spectral mask, or for envelope tracking systems [5] where the ripple and accuracy of the modulator is less important. Efficient supply modulation is also reported for a hybrid polar and envelope tracking amplifier [6], but the spectral mask compliance is unclear. The major requirements of the supply modulator used in a polar modulation architecture are large bandwidth, low switching ripple and small differential delay between envelope and phase paths. Similarly for the RF power amplifier, feed-through and nonlinear drain-source capacitance of the output transistor are the two main challenges for implementation. This chapter describes the details of the challenges and prototype implementation of a polar modulated power amplifier along with several techniques to overcome those problems. The prototype is implemented for a WLAN IEEE 802.11g 64QAM OFDM standard as its signal has large bandwidth (20MHz) and high peak to average power ratio (~10dB), hence a difficult standard for implementation. In addition, this chapter presents a detailed theoretical analysis and derives critical parameters for the design with an extensive discussion on design choices.

The remainder of this paper is organized as follows. Section 4.1 elaborates on the challenges of polar modulated amplifiers. In section 4.2, an overview of the operation of supply modulator is then given. System level design choices and optimization techniques are also discussed in this section. The implementation of the supply modulator is discussed in section 4.3. In section 4.4, the design and implementation of the class-E RF power amplifier is described. Section 4.5 presents the measurement results obtained for the polar amplifier module prototype and finally, conclusions are drawn in section 4.6. This chapter is based on our publications [7], [8].

4.1 Challenges of Polar Modulated Power Amplifiers

4.1.1 Bandwidth of Supply Modulator

The signal representing the envelope of a complex modulated RF signal has a much higher bandwidth than the bandwidth of the rf signal itself [9]. For example, consider a two tone signal with carrier frequency, ω_c and modulation frequency ω_m,

$$v_i(t) = \cos\omega_m t \times \cos\omega_c t = \left|\cos\omega_m t\right| \cos(\omega_c t + \phi_i t) \qquad 4.1$$

Where $\varphi_i(t) = \begin{cases} 0, & \cos\omega_m t \geq 0 \\ \pi, & \cos\omega_m t \leq 0 \end{cases}$ (1)

The signal $v_i(t)$ has an RF signal bandwidth of $2\omega_m$. But the envelope of $v_i(t)$, $\left|\cos\omega_m t\right|$, contains frequency components at dc, $2\omega_m, 4\omega_m, 6\omega_m, 8\omega_m$ …..etc. Since a typical modulator has a first order low pass frequency response in its modulation frequency band, the bandwidth of the modulator used in a polar transmitter should be at least 5 or 6 times higher than the signal bandwidth to avoid significant distortion. Figure 4.2 shows the effect of Modulator bandwidth on EVM for the IEEE 802.11g WLAN OFDM signal, which has 20MHz signal bandwidth, considering all other components in the polar modulator system ideal. The distortion in this case is contributed only by the modulator

having a first order low pass frequency response. EVM deteriorates rapidly as the modulator bandwidth decreased below about 100MHz. The maximum allowed EVM for IEEE 802.11g signal is 5.6% (at 54Mbps data rate).

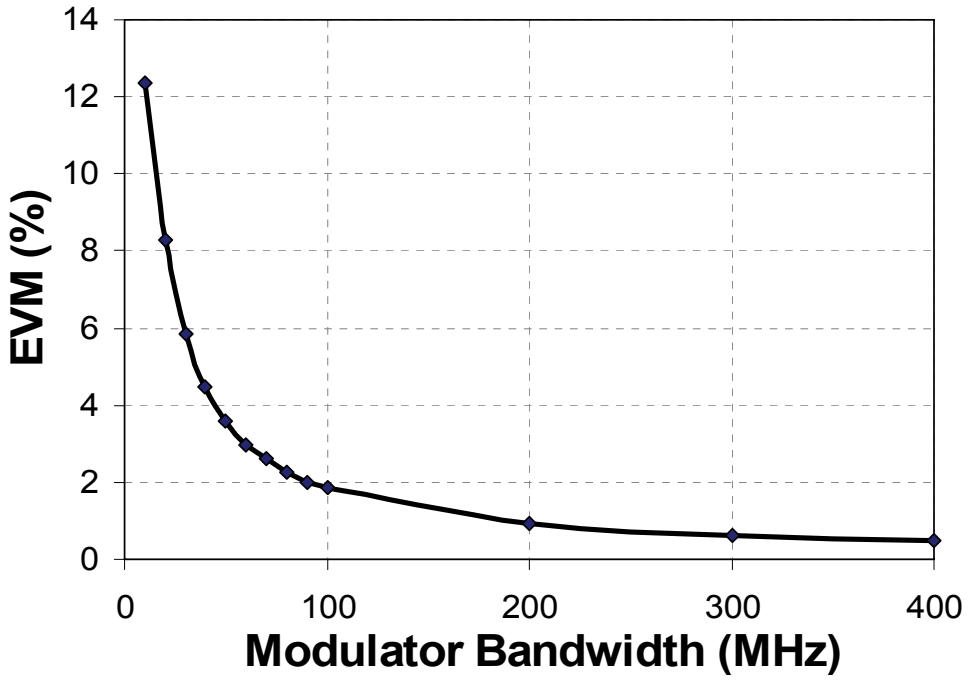


Figure 4.2 Simulated EVM versus modulator bandwidth for WLAN IEEE 802.11g OFDM signal

4.1.2 Differential delay between envelope and phase paths

Differential delay between envelope and phase paths is another problem. A conventional buck converter for the supply modulator suffers from a large delay compared to the phase path because of the (passive) output filter. This affects the linearity of the polar modulated system. For example, consider a two tone signal of equation 4.1. The equation can rewritten as

$$v_i(t) = \left|\cos \omega_m t\right| \cdot c(\theta) \cdot \cos(\omega_c t) = f(\theta)\cos(\omega_c t) \qquad 4.2$$

Where $c(\theta)$ is a phase function and $f(\theta)$ is a modulating function.

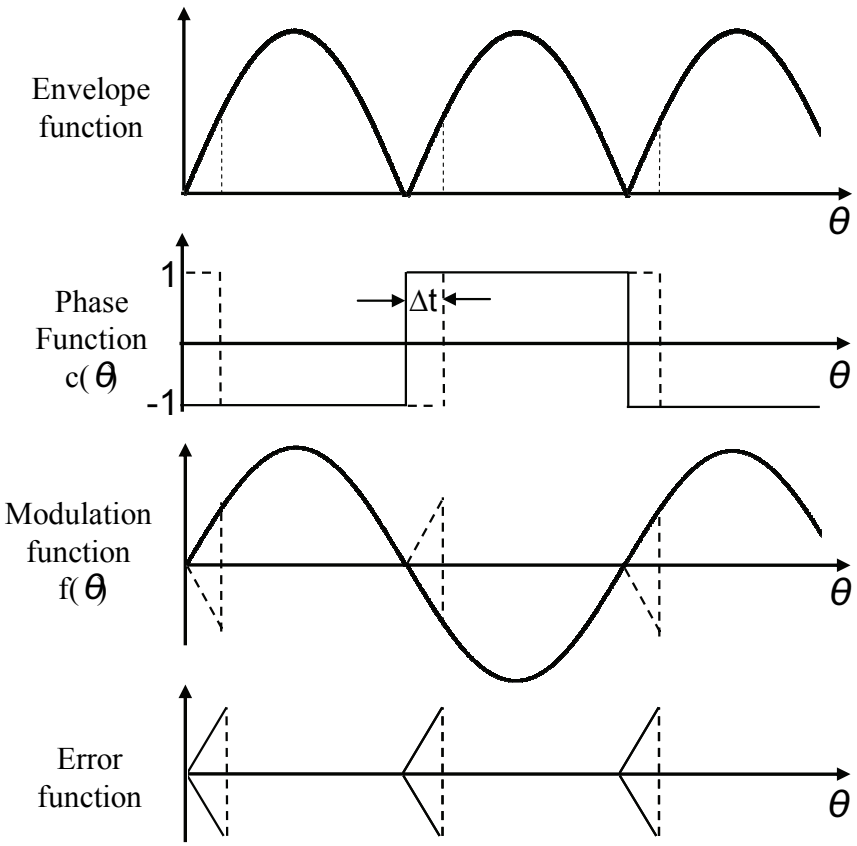


Figure 4.3 Waveforms showing the effect of differential delay with a two-tone signal

Figure 4.3 shows the waveforms of a two-tone signal illustrating the effect of differential delay between the envelope and the phase path. Here the delay is represented by the delay in phase function. The delay causes the unnecessary inversion of the polarity of modulation function and hence it will not be sinusoidal anymore. The error function in the presence of the delay is also shown in the figure. The resulting intermodulation distortion as a function of differential delay is derived in [9] and is given by

$$S_{IMD} = \pi(\Delta t.B_{rf})^2 \qquad 4.3$$

Where B_{rf} is the RF signal bandwidth and Δt is the differential delay

This equation also shows that the effect of delay mismatch is worse for standards with a large RF bandwidth. Figure 4.4 shows the effect of delay mismatch on EVM of a IEEE 802.11g WLAN OFDM signal considering that distortion is only contributed by the delay mismatch. Even for 1ns of delay mismatch, EVM gets worse by more than 1.2%. This is a significant proportion of the maximum allowed EVM of 5.6% for IEEE 802.11g, when the distortion contribution by various sources like AM-PM/AM-AM conversion of the RF PA, bandwidth limitation of the modulator, bandwidth limitation of the baseband signal generator, and memory effects in the PA drivers are added.

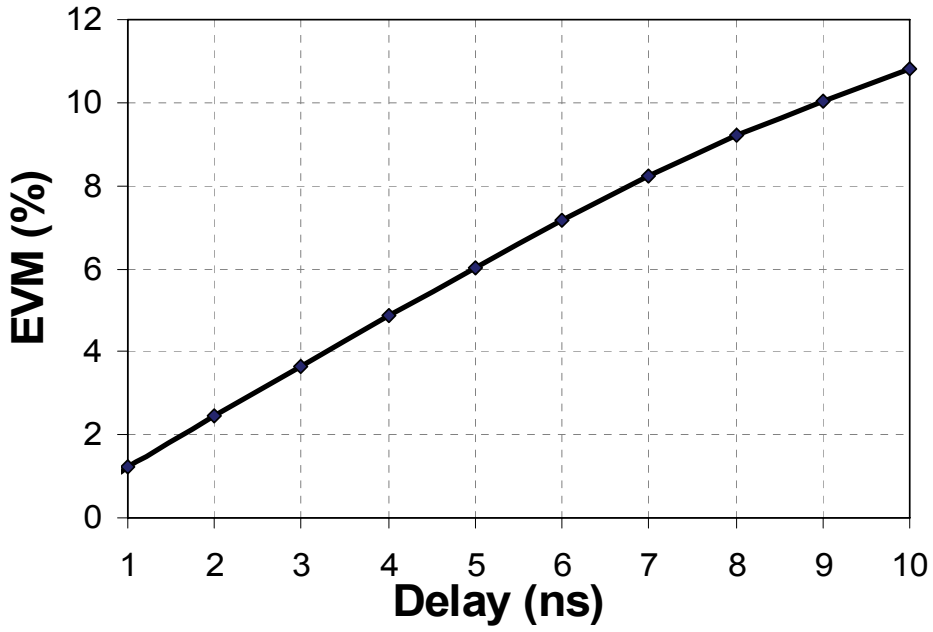


Figure 4.4 Simulated EVM versus differential delay between envelope and phase paths for WLAN IEEE 802.11g OFDM signal

4.1.3 Switching Noise of the Supply Modulator

Since any switching noise in the supply modulator will appear directly at the antenna, it should be small enough to satisfy the spurious emission requirements. This requirement can be relaxed by the use of envelope tracking, where the PA supply voltage only tracks the envelope. However it uses a less efficient linear RF amplifier whereas polar modulation uses a saturated amplifier which has a higher efficiency. The detailed discussion of the switching noise problem is given in section 4.2 and 4.3.

4.1.4 Feed-through

Ideally, the output signal amplitude of the switching power amplifier is proportional to its supply voltage and the phase is constant. But in practice the conversion is imperfect by other effects such as nonlinearity and is characterized by AM-AM (Vdd-to-amplitude) and AM-PM (Vdd-to-phase) distortions. One of the main sources of AM-AM and AM-PM conversion is a feed-through from the gate terminal of the final PA to the output via the gate-drain capacitance. In this sub-section, we investigate the effect of feed-through in a class-E power amplifier used in the polar amplifier system.

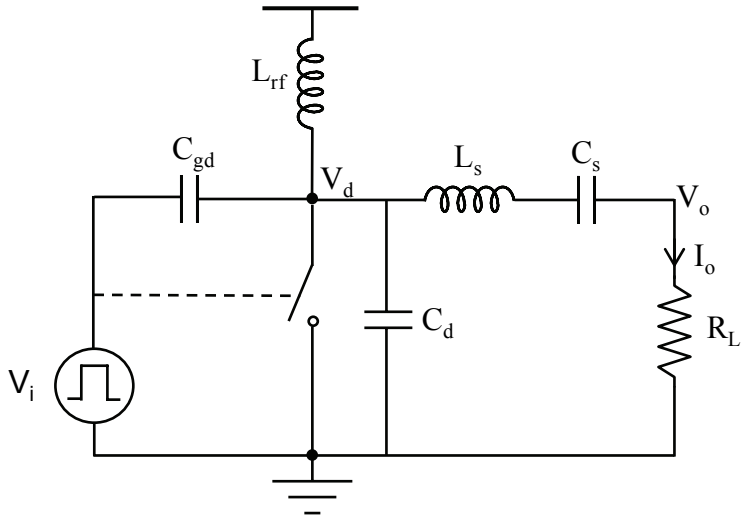


Figure 4.5 Class E PA with feed-through from C_{gd}

Figure 4.5 shows the class-E power amplifier where C_{gd} represents the feed-through capacitance. Assuming 100% power efficiency, the drain voltage waveforms of the class-E amplifier as derived in [10] is given by

$$V_d(\theta) = \pi V_{dd}(\theta + \frac{\pi}{2}\cos\theta + \sin\theta - \frac{\pi}{2}) \qquad 4.4$$

Where $\theta = \omega t$. Note that equation 4.4 is without the effect of C_{gd}. By using the Fourier transform, the magnitude of the fundamental frequency of the drain voltage waveform becomes

$$|V_d| = \frac{1}{\pi}\sqrt{\left(\int_0^{\pi} V_d(\theta)\sin\theta.d\theta\right)^2 + \left(\int_0^{\pi} V_d(\theta)\cos\theta.d\theta\right)^2} = 1.639V_{dd} \qquad 4.5$$

The fundamental component of the feed-through current is

$$I_{ft}(\omega) = j\omega C_{gd}[V_d(\omega) - V_i(\omega)] \qquad 4.6$$

The fundamental output current without feed-through effect can be calculated as

$$I_{om}(\omega) = \frac{V_d(\omega)}{\sqrt{R_L^2 + X^2}} \qquad 4.7$$

Where $X = \left(\omega L_s - \frac{1}{\omega C_s}\right)$

The fundamental component of the total output current is

$$I_0(\omega) = I_{fi}(\omega) + I_{om}(\omega) = V_d(\omega)\left(\frac{1}{\sqrt{R_L^2 + X^2}} + j\omega C_{gd}\right) - j\omega C_{gd} V_i(\omega) \qquad 4.8$$

Since $\frac{1}{\sqrt{R_L^2 + X^2}} >> j\omega C_{gd}$, equation 4.8 can be rewritten as

$$I_0(\omega) = \frac{V_d(\omega)}{\sqrt{R_L^2 + X^2}} - j\omega C_{gd} V_i(\omega) \qquad 4.9$$

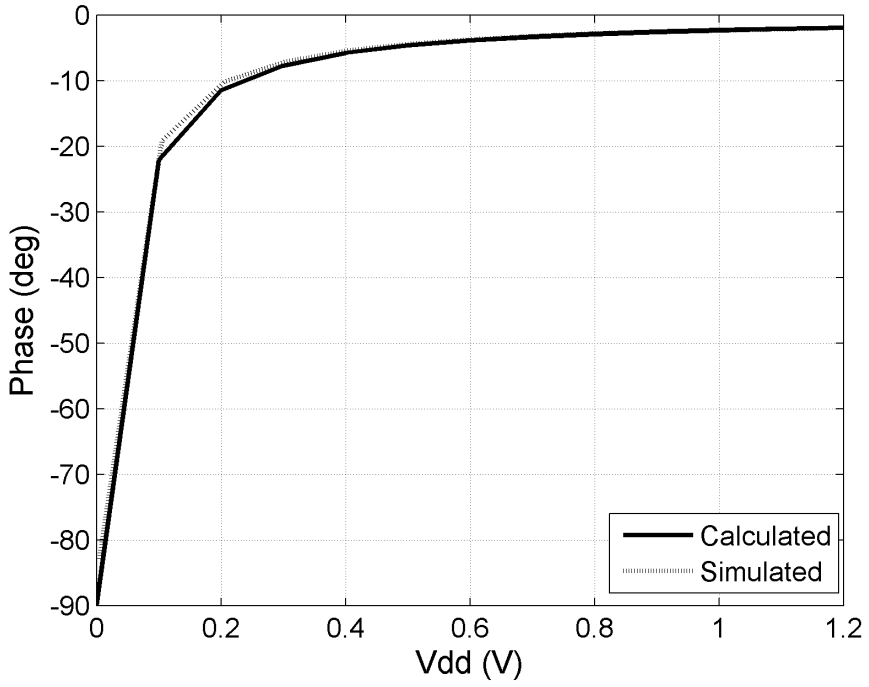
Since $|V_d(\omega)| = 1.639 V_{dd}$ and $|V_i(\omega)| = \frac{V_{ih}}{2}$, where V_{ih} is the upper level of the square wave (lower level=0V), the magnitude and the (relative) phase of the fundamental output current is given by

$$|I_o| = \sqrt{\frac{2.686 V_{dd}^2}{R_L^2 + X^2} + \left(\frac{\omega C_{gd} V_{ih}}{2}\right)^2} \qquad 4.10$$

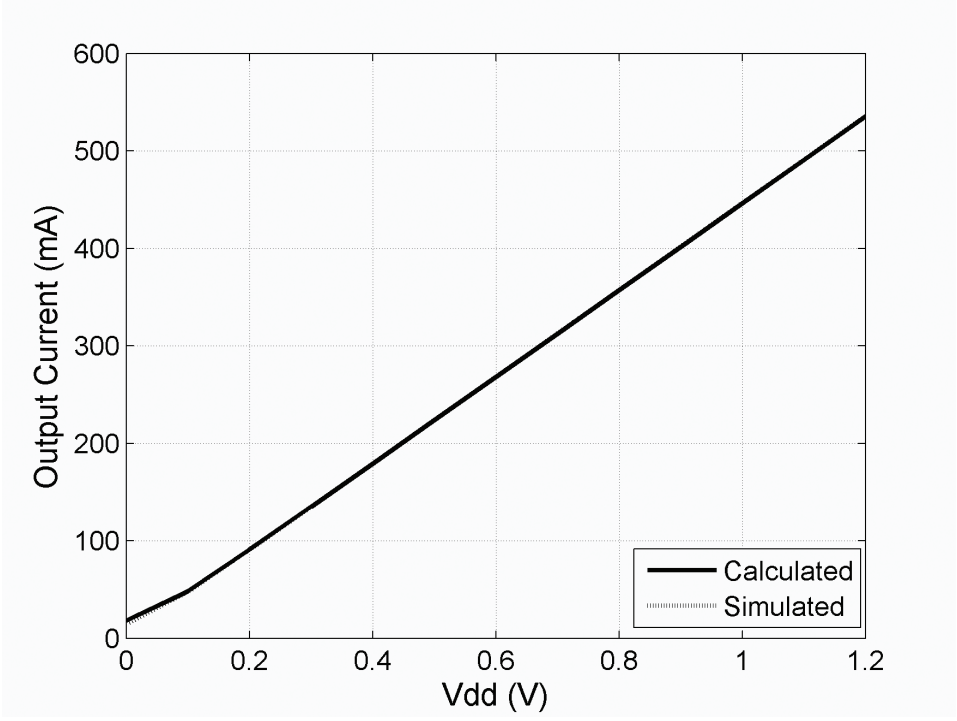
$$\angle I_o = \tan^{-1}\left(-\frac{\omega C_{gd} V_{ih}\sqrt{R_L^2 + X^2}}{3.278 V_{dd}}\right) \qquad 4.11$$

Example

As an example to validate above calculations, a class-E amplifier operating at 2.4GHz with the targeted output power of 350mW at V_{dd}=1.2V is designed and simulated. Class-E operation is achieved with the component values: L_s=1.02nH, C_s=5.3pF, C_d=6pF and R_L=2.3Ω in Figure 4.5. Note that when C_{gd} is added, the value of C_d might need to be changed to obtain zero voltage switching. Figure 4.6 shows the magnitude and phase of the fundamental output with C_{gd}=2pF and V_{ih}=1.2V, calculated using equations 4.10 and 4.11. The simulated result of Figure 4.5 is also shown. The circuit is simulated using the Spectre circuit simulator. In the simulation, an ON-resistance of 1mΩ to aid the convergence and a modified C_d of 4pF are used. The figure shows that the calculated AM-PM and AM-AM conversion using equations 4.10 and 4.11 is very well matched with the simulation. The power delivered was 330mW at V_{dd}=1.2V.



(a)



(b)

Figure 4.6 Calculated and simulated (a) AM-PM and (b) AM-AM conversion for C_{gd}=2pF

Equation 4.9 and the above example show that the effect of feed-through current on distortion is significant at lower supply voltages. AM-PM distortion is particularly high in the whole range of supply voltage variations, whereas AM-AM distortion is visible as V_{dd} tends to zero.

4.1.5 Nonlinear Parasitic Output Capacitance

Another source of AM-PM and AM-AM distortion in the polar modulated power amplifier is the non-linear drain-bulk junction capacitance. As the drain-source voltage increases, the depletion region at the reverse biased drain-bulk junction also increases and hence the drain-bulk junction (drain-source) capacitance decreases or vice versa. As a result the phase of the output signal of the PA is not constant to its supply voltage variations. It also causes AM-AM distortion but it is less visible. The variation of the drain-bulk junction capacitance can be expressed as [10]:

$$C_{jdb} = \frac{C_{jo}}{\left(1+\frac{v}{V_{bi}}\right)^{m}} \qquad 4.12$$

Where C_{jo} is the zero-bias capacitance, v is the reverse voltage over the junction, V_{bi} is the built-in voltage of the junction and m is the grading coefficient such that m<1. A step profile junction has m=0.5, while a linearly graded junction has m=0.33.

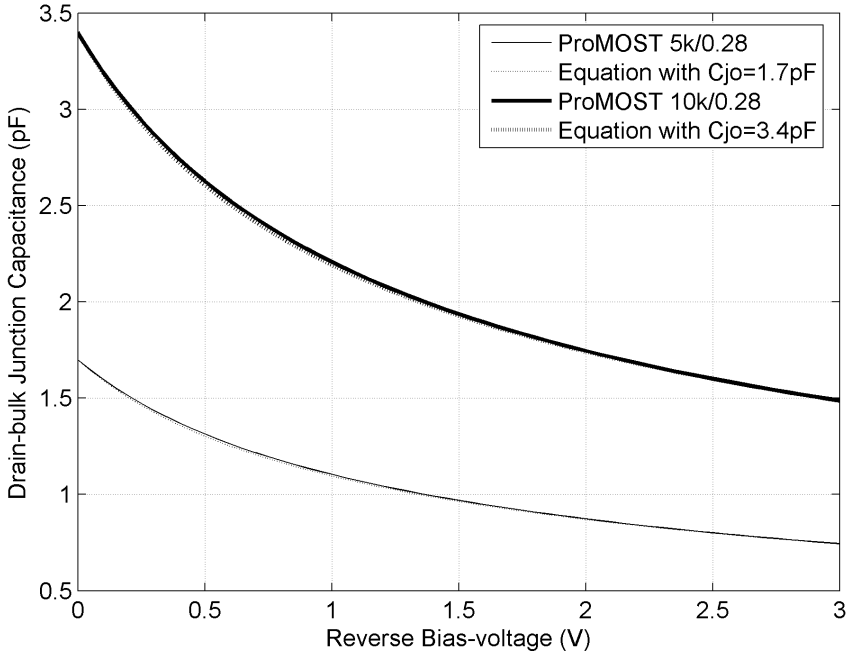


Figure 4.7 Drain-bulk junction capacitance of the thick oxide transistor in 65nm CMOS

Figure 4.7 shows the drain-bulk junction capacitance of the thick oxide transistor in 65nm CMOS technology, simulated in ProMOST [11] as a function of the reverse bias-voltage. The figure also shows the variation of the drain-bulk capacitance according to equation 4.12 for C_{jo}=1.7pF and 3.4pF with m=0.5 and V_{bi}=0.71V. Typically, the shunt capacitance of the class-E amplifier is composed of the drain-source (bulk) capacitance in parallel with a linear capacitor. The phase variation due to the nonlinear drain-source capacitance is illustrated in the following example.

Example

A class-E amplifier operating at 2.4GHz with the targeted output power of 140mW at V_{dd}=1.2V is designed. Class-E operation is achieved with the component values: L_s=2.74nH, C_s=1.95pF, and R_L=5.9Ω. C_d is composed of the linear capacitor of 1.4pF and the nonlinear capacitor modeled by equation 4.12 with C_{jo}=1.7pF, m=0.5 and V_{bi}=0.71V. The nonlinear capacitor is modeled in Verilog-A and the circuit is simulated in the Spectre circuit simulator. The switch is assumed ideal and C_{gd}=0. The plot of the output phase against the supply voltage is shown in the Figure 4.8. It shows that the AM-PM distortion is significant due to the non-linear drain-bulk junction capacitance.

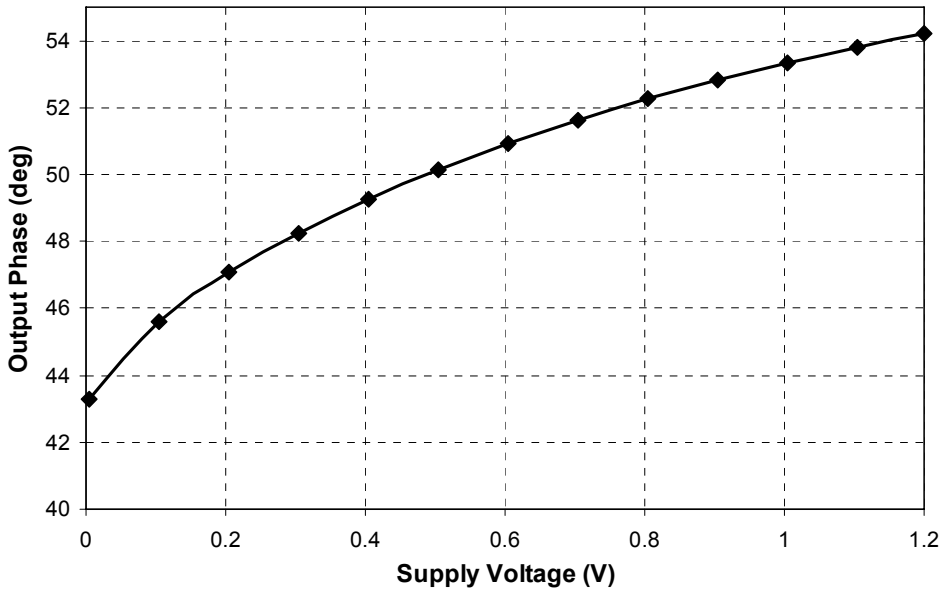


Figure 4.8 Output phase variation as function of the supply voltage due to nonlinear drain-source capacitance

Further note that the relative phase decreases as the supply voltage decrease in Figure 4.8. In the case of the presence of feed-through capacitor in Figure 4.6 (a) the phase change is also in the same way as the function of its supply voltage. This means that the phase distortion due to the nonlinear drain-source capacitor and the feed-through capacitor are added up for the worst.

4.1.6 Conclusion

Key problems for the implementation of polar modulated power amplifiers are bandwidth of the supply modulator, differential delay between the envelope and phase paths, switching noise of the supply modulator, feed-through in the RF PA and nonlinear parasitic output capacitance. The first three problems are related to the supply modulator. The other two problems are related to the RF power amplifier.

4.2 Supply Modulator Design

The key building block of the polar amplifier is the supply modulator. At the start of this section an overview of the operation of the hybrid supply modulator comprising of a linear and switching amplifier is given. The remaining part of the section focuses on the system level design issues.

4.2.1 Overview of Operation

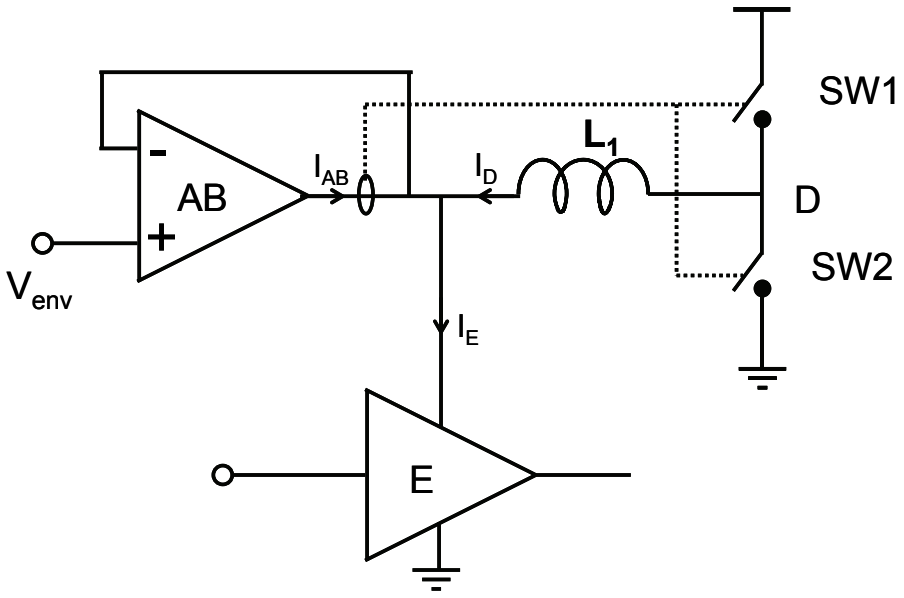


Figure 4.9 Schematic of the Modulator combining linear and switching amplifier

Figure 4.9 shows the architecture of the modulator comprising a self oscillating parallel linear and switching amplifier [1], [4], [6], [7], [8], [12]. The linear amplifier (AB) takes care of the linearity while the switching amplifier (D) supplies most of the current ensuring high efficiency. The amplifier AB is used in feedback mode not only to reproduce the input envelope with low distortion but also to attenuate the switching ripple of switching amplifier D. The control signal for the switching part is derived by copying the output current of AB and comparing it with a threshold level using a hysteretic comparator as shown in Figure 4.10. When switch SW1 is closed, and SW2 is open, the current through L1 increases linearly with time and the unwanted part of the load current flows into AB. When this current exceeds a certain threshold value SW1 is opened, and

SW2 is closed. Then the current through L_1 decreases and so on. Since the current through AB oscillates between two small threshold currents the power dissipation in the linear part is small, while switching part D delivers most of the load current and the AB-D system is self-oscillating with a frequency inversely proportional to the hysteresis. Since the delay in the supply modulator from input-to-output only depends on AB, the differential delay between the envelope and phase paths can be matched.

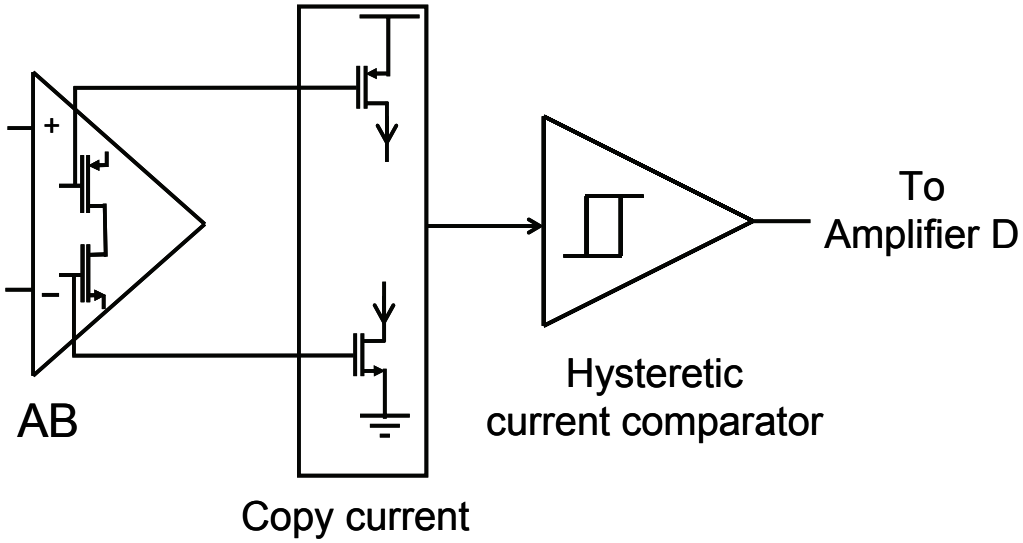


Figure 4.10 Schematic of sense and control circuit

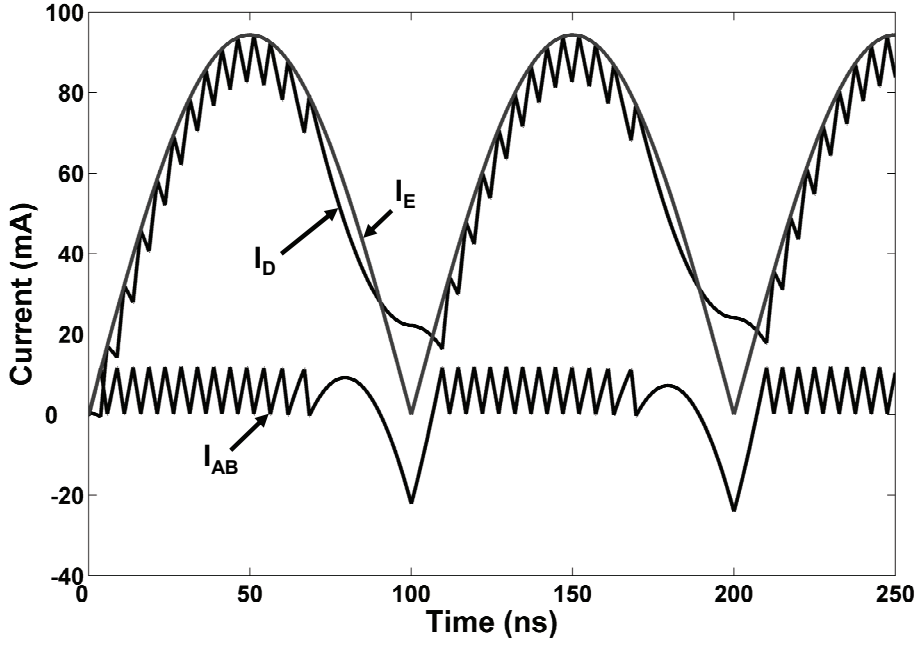


Figure 4.11 Current supplied by the AB and D amplifier to the load

Figure 4.11 shows the output current I_E supplied to the PA, and the currents supplied by the class D and AB amplifiers for a full wave rectified signal of 10MHz sine-wave input voltage of $0.5V_{peak}$ and a load resistance of 5.3Ω. This value of load resistance is chosen considering the design for IEEE 802.11g WLAN OFDM signal applications and the reason is as follows: To have a 12dBm average output power for the WLAN signal at the antenna, the peak RF output power should be about 21dBm considering 10dB PAPR and 1dB clip. If we assume the RF PA has 50% efficiency then the supply modulator should be able to supply about 250mW peak power. This means the equivalent load resistance of the modulator is about 5.3Ω when the supply modulator reaches the maximum output voltage of 1.15V from a 1.2V supply.

4.2.2 IEEE 802.11g WLAN Signal

Since we aim to implement the supply modulator for IEEE 802.11g WLAN standard, some relevant basics of the standard is discussed in this subsection. The WLAN IEEE 802.11g OFDM system provides a wireless LAN with data transmission capabilities of 6, 9, 12, 18, 24, 36, 48, and 54 Mbps. The system operates in the 2.4GHz ISM band and uses 52 subcarriers that are modulated using BPSK or QPSK or 16-QAM, or 64-QAM. Out of 52 subcarriers, four of the subcarriers are dedicated to pilot signals in order to make the coherent detection robust against frequency offset and phase noise. 48 subcarriers are for data. So the transmitted signal can carry up to 288 coded bits (6 bits/carrier using 64-QAM modulation) per OFDM symbol.

The WLAN IEEE 802.11g signal bursts are separated by an idle interval and composed of the Short Preamble, Long Preamble, SIGNAL and DATA fields [13], [14]. The signal bandwidth is 20MHz, resulting in OFDM symbol duration of 4us. SIGNAL contains information such as data rate, payload data, and length. DATA contains payload data.

The time domain envelope of one complete burst is shown in Figure 4.12 as an example. The initial 4us interval is the idle time when the transmitter sends no signal, and follows the short preamble, long preamble, SIGNAL and DATA fields. Short and Long preamble are each 8us long, lasting from 4 to 12us and from 12 to 20us respectively in Figure 4.12. The SIGNAL is 4us lasting from 20 to 24us. Remaining 76us, lasting from 24us to 100us, is time duration for DATA. The RF signal has a PAPR of 11.76dB, peak envelope voltage of 1.28V and average envelope voltage of 0.33V excluding the idle interval.

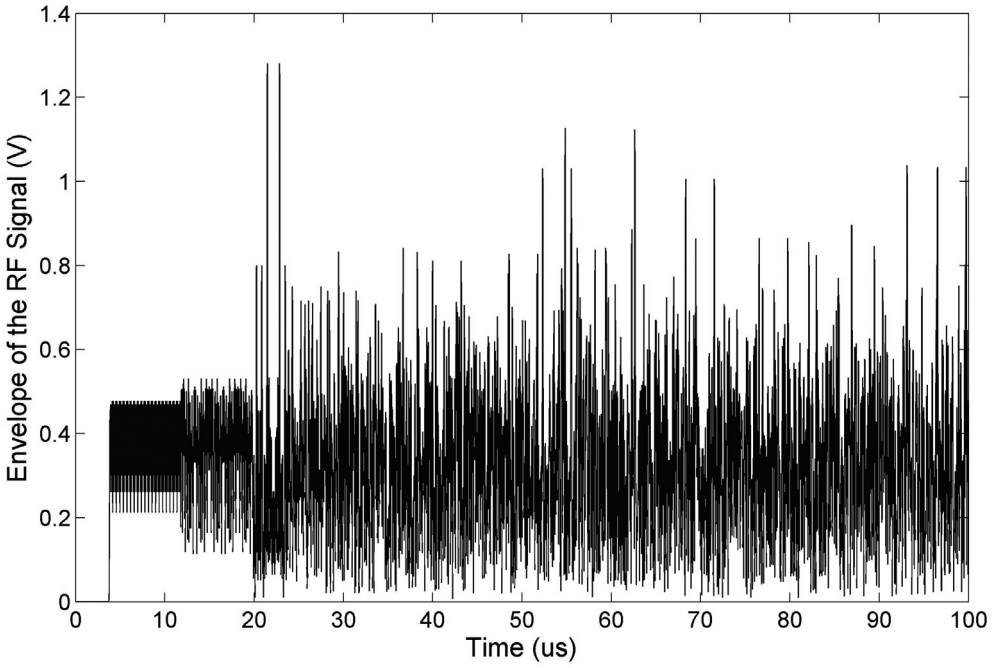


Figure 4.12 Time Envelope of one complete WLANa/g RF signal burst of 100us

Figure 4.13 shows the probability density function of the signal normalized to 0dBm average output power. The probability density is the highest in the region of ~0.5 to ~3.5dBm above the average output power.

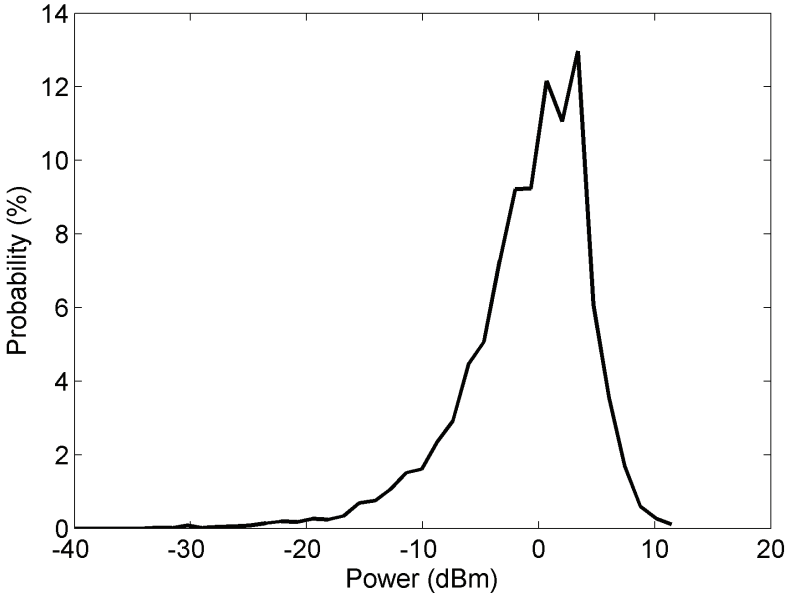


Figure 4.13: Probability Density Function of the WLANa/g signal of Figure 4.12.

4.2.3 Switching Frequency

The previous subsection briefly describes the characteristic of the WLAN signal. This subsection will discuss the switching frequency characteristic of the supply modulator of Figure 4.9.

If the upper and lower thresholds current levels of AB are I_{thrH} and $I_{thrL,}$ and the threshold current $I_{thr} = (It_{hrH}\text{-}I_{thrL})/2$, then the oscillation frequency as derived in [12] is given by:

$$f_{sw} = \frac{V_{dd}\left[V_o + \frac{L_1}{R_{PA}}\frac{dV_o}{dt}\right] - \left[V_o + \frac{L_1}{R_{PA}}\frac{dV_o}{dt}\right]^2}{2L_1 I_{thr} V_{dd}} \qquad 4.13$$

Where R_{PA} is the load seen from the supply side, and V_o is the -time dependent- envelope voltage or the supply voltage for the RF PA.

The switching frequency depends on the choice of L_1 and I_{thr}. It also varies with the envelope voltage and/or its slope. From equation 4.13, the switching frequency for a dc envelope is given by,

$$f_{sw,dc} = \frac{V_{dd}V_o - V_o^2}{2L_1 I_{thr} V_{dd}} \qquad 4.14$$

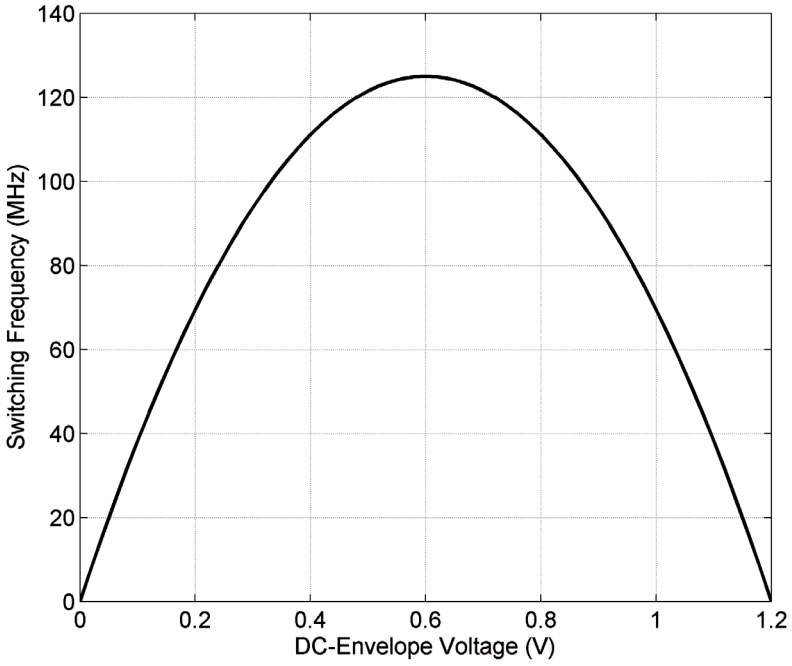


Figure 4.14 Switching frequency of a modulator for a DC-Envelope input

Figure 4.14 shows the plot of the switching frequency for the DC input (envelope) voltage. The plot is for V_{dd}=1.2V, L_1=80nH and I_{thr}=15mA. The switching frequency is the highest when the envelope voltage is dc with a magnitude of $V_{dd}/2$. This maximum switching frequency is given by,

$$f_{sw,\max} = \frac{V_{dd}}{8L_1 I_{thr}} \tag{4.15}$$

As described above, the switching frequency depends on many parameters; L_1, I_{thr}, envelope voltage and/or its slope. The choice of L_1 and I_{thr} will be discussed in the following subsections. It is interesting to see the distribution of switching frequencies in the case of a true signal. When the main frequency band of spurs falls to adjacent channels, it is very difficult, if not impossible, to satisfy the switching ripple requirements in many cellular applications. However, the design of the modulator can be optimized to tune the spurs to areas in the spectrum where the requirements are less stringent. So it is important to understand the behavior of the switching frequency. For this the WLAN IEEE 802.11g signal is applied to the input of an ideal modulator consisting of the linear and switching amplifiers. The signal has the PAPR of 9dB, peak envelope voltage of 1.2V and average envelope voltage of 0.426V. Similarly, V_{dd}=1.2V, L_1=80nH and I_{thr}=15mA are chosen in this example. A histogram plot of the distribution of instantaneous switching frequency is shown in Figure 4.15. The maximum switching frequency is 125MHz. The highest number of counts is at the maximum switching frequency. Note that the shape of the histogram changes when the average envelope (RF) power decreases. However the switching frequency histogram at the highest average RF power is more important because the ripple is worst in this case.

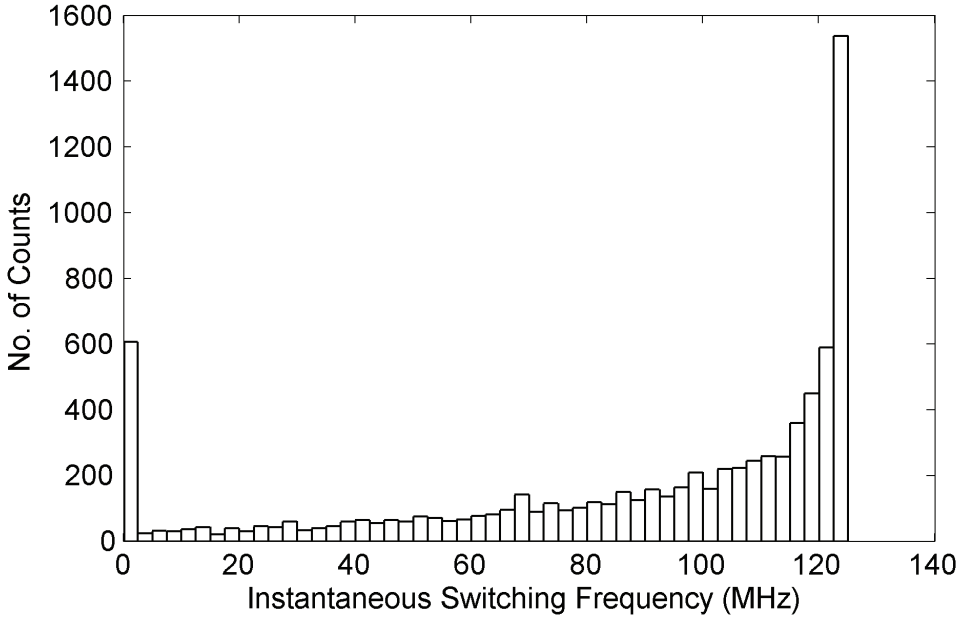


Figure 4.15: A histogram of the instantaneous switching frequency of D for the WLAN signal

4.2.4 Dissipation

The choice of L_1 depends primarily on the envelope bandwidth and power dissipation in the linear amplifier. When L_1 is chosen large, the switching amplifier cannot deliver a large current at high frequencies, so the linear amplifier has to deliver the remaining part leading to a higher dissipation. Similarly a low value of L_1 will result in a high power bandwidth of the class D amplifier, but also in a high switching frequency. A high switching frequency means a high switching loss in the class D amplifier. For a compact design, the resistive power dissipation in L_1 is also significant. So the choice of L_1 also depends on its parasitic series resistance. When L_1 is chosen large, the series resistance also gets larger, and so will the dissipation.

The choice of I_{thr} depends on the power dissipation in AB and D. When I_{thr} is chosen large, the dissipation in AB increases. Similarly when I_{thr} is chosen small, the switching frequency becomes high which results in high switching losses.

4.2.5 First Order Model for Efficiency Optimization

Since the switching frequency also depends on the instantaneous envelope voltage and its slew rate, the choice of L_1 and I_{thr} as discussed in Section 4.2.4 for the optimum efficiency of the modulator is complicated. It has to be noted that the optimum L_1 and I_{thr} is valid for only one value of envelope voltage and slew rate.

Let's consider the case where the envelope is dc. In this case AB is supplying only the switching ripple current. Assuming that the class AB amplifier is ideal and its dissipation is only in the output stage, the dissipation in AB due to this switching current is given by,

$$P_{ABsw} = \frac{1}{2} I_{thr} . V_{dd} \qquad 4.16$$

Assuming that the series resistance of the coil varies proportionally to the inductance, the power dissipation in the coil is given by,

$$P_{L1} = I^2 a_{L1} L_1 \qquad 4.17$$

where a_{L1} is the resistance per Henry of inductance, and I is the average output current of D.

The output node of the class D amplifier has a parasitic capacitance. A square voltage wave across this capacitance results in capacitive dissipation which is proportional to the switching frequency. However for each switching frequency the size of the power stage of D can be optimized such that the sum of resistive and capacitive dissipation is minimized. For an optimally sized output stage, the dissipation of D is given by (see section 4.3.2):

$$P_D = 2 V_{dd} I \sqrt{f R_{eq} C_{eq}} \qquad 4.18$$

where R_{eq} is the equivalent on-resistance and C_{eq} is the total equivalent capacitance of the output stage of D, which will be further discussed in section 4.3.2.

The sum of the power dissipation in AB, D and the coil from equation 4.15, 4.16, 4.17, and 4.18 is given by,

$$P_{diss} = \frac{1}{2} I_{thr} . V_{dd} + I^2 a_{L1} L_1 + 2 V_{dd} I \sqrt{\frac{V_{dd} (\alpha - \alpha^2) R_{eq} C_{eq}}{2 L_1 I_{thr}}} \qquad 4.19$$

where $\alpha = \frac{V_o}{V_{dd}}$, the amplitude as a fraction of V_{dd}.

The optimum values of I_{thr} and L_1 that minimize the total power dissipation, P_{diss}, can be found by setting the first partial derivative of equation 4.19 to zero $\left(\frac{\partial P_{diss}}{\partial I_{thr}} = 0 \text{ and } \frac{\partial P_{diss}}{\partial L_1} = 0 \right)$. This leads to

$$I_{thr} = I \left[4(\alpha - \alpha^2) R_{eq} C_{eq} a_{L1} \right]^{\frac{1}{4}} \qquad 4.20$$

$$L_1 = \frac{V_{dd}}{2 I a_L} [4(\alpha - \alpha^2) R_{eq} C_{eq} a_{L1}]^{\frac{1}{4}} \qquad 4.21$$

The power dissipation in these conditions is

$$P_{dis} = 4 V_{dd} I [(\alpha - \alpha^2) R_{eq} C_{eq} \frac{a_{L1}}{4}]^{\frac{1}{4}} \qquad 4.22$$

Equations 4.20 and 4.21 are derived for a DC envelope signal. Now we have to investigate whether 4.20 and 4.21 are valid for a true WLAN OFDM signal. Figure 4.16(a) shows the simulated spectrum of the amplitude of the IEEE 802.11g WLAN OFDM signal. For this envelope signal most of the energy is at dc as shown in Figure 4.16(b). Simulation results show that more than 75% of the energy is concentrated between DC and 250kHz. This suggests that, for high switching frequencies, the effect of envelope slewing can be neglected as far as efficiency is concerned. In other words equation 4.20 and 4.21 can be used to get a first estimation of L_1 and I_{thr} for the optimum efficiency.

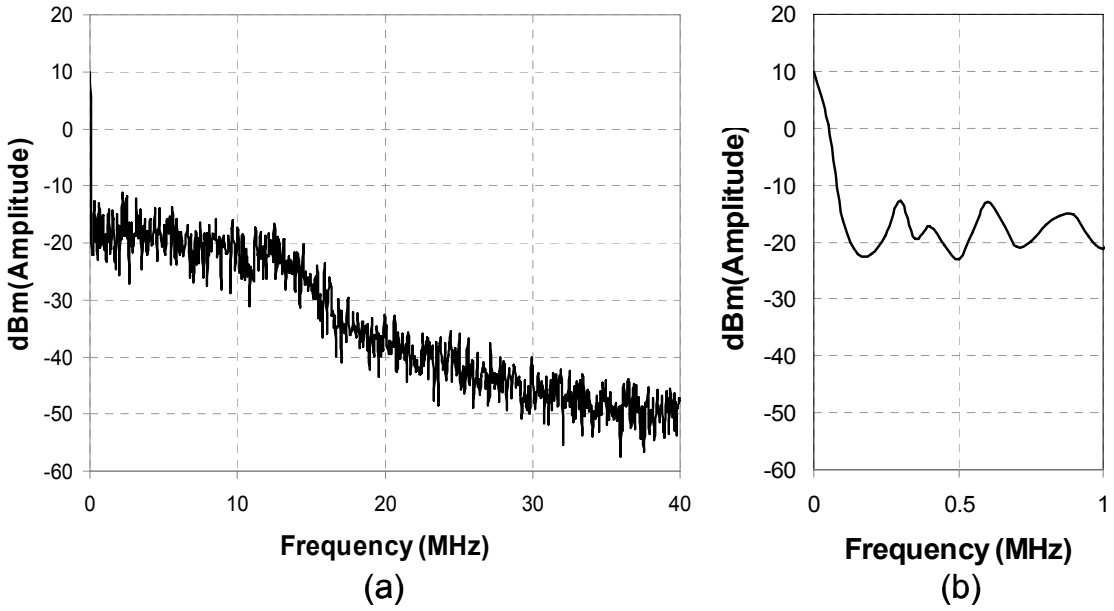


Figure 4.16 (a) Spectrum of WLAN 802.11g OFDM signal envelope (amplitude), (b) Detailed spectrum around DC

To further justify the use of equation 4.20 and 4.21 for a true signal, we compare two first order designs of a modulator; one by using those equations neglecting the slewing effect and another with the WLAN signal. In case of hard switching of D, we get $R_{eq}C_{eq}=3.94\times10^{-12}$ ΩF for 65nm CMOS using minimal channel length transistors. For I=90mA and α=.5 and V_{dd}=1.2V, a_{L1}=5mΩ/nH, optimum efficiency is obtained when I_{thr}=6mA and L_1=89nH from equation 4.20 and 4.21. The resulting switching frequency is about 281MHz. Here the optimization is done at the dc output voltage of $V_{dd}/2$ (i.e. α=0.5). The reason for this is given in section 4.3.2.

Figure 4.17 shows an example plot of the total power dissipation in D, L_1 and AB calculated using the equation 4.19 for the IEEE 802.11g WLAN signal at the output. Since it is allowed to have some clipping of the signal to maximize the efficiency while still satisfying the linearity requirements, the signal has the PAPR of 9dB and the average envelope voltage of 0.426V after clipping. In Figure 4.17 the instantaneous power dissipation is calculated at each point of the signal, and then summed up to get the total power dissipation by using Matlab. The calculation is repeated for different values of I_{thr} and L_1. The corresponding switching frequency is plotted in Figure 4.18. The optimum I_{thr} and L_1 from Figure 4.17 are 5mA and 95nH respectively. This is close to the predicted optimum point (I_{thr}=6mA and L_1=89nH) from equation 4.20 and 4.21.

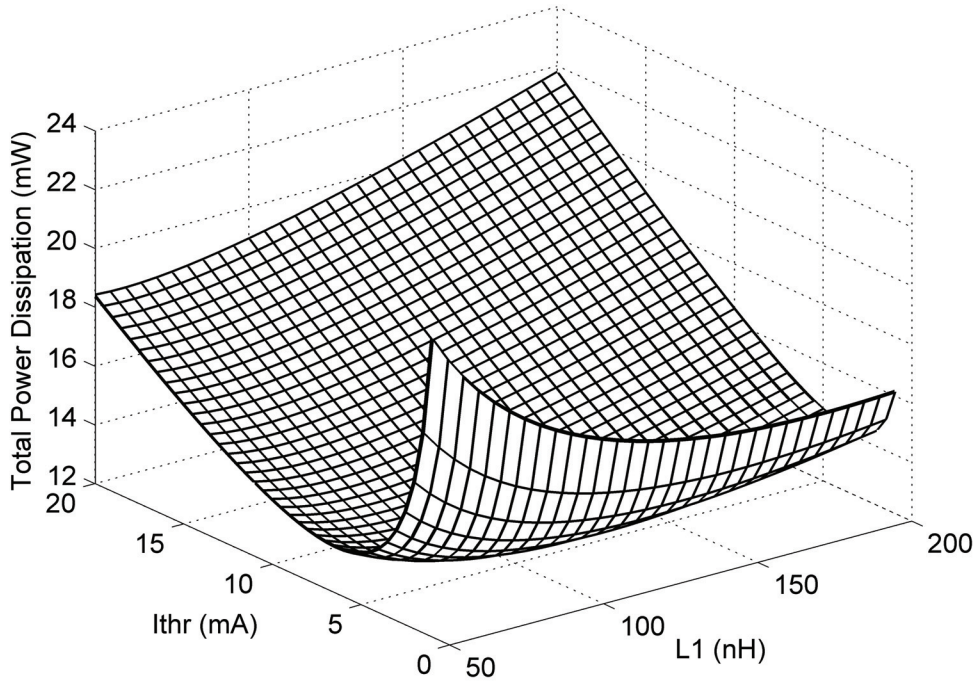


Figure 4.17: Power Dissipation in a modulator for a IEEE 802.11 WLANa/g signal output, assuming the losses are mainly on the output stage of D, L1 and AB

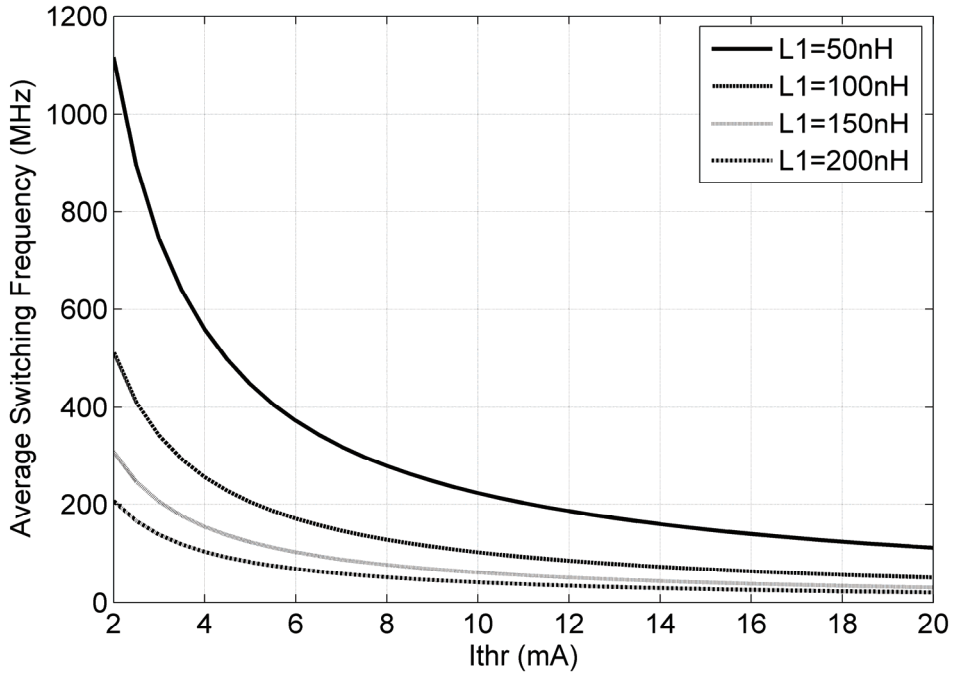


Figure 4.18: Switching Frequency of D for a IEEE 802.11 WLANa/g signal output

However, the maximum switching frequency in the above design is 281MHz. At this frequency it is very hard to achieve enough loop gain for low Z_o of AB (see section 4.2.6). So the switching frequency has to be decreased. Since we prefer to have a small inductor value for a large power bandwidth of D and compactness, L_1 and I_{thr} is chosen 80nH and ~15mA respectively. The corresponding switching frequency is 125MHz for a dc envelope. The average switching frequency is 89MHz and the maximum switching frequency is 125MHz for the WLAN OFDM signal, when the effect of high frequency content included.

4.2.6 Switching Residue

The choice of L_1 and I_{thr} also has consequences on the switching residue. Because of the low frequency pole, the loop gain of AB has a first order behavior. So for frequencies higher than the pole frequency, the loop gain will have a first order roll off, which leads to an apparent inductive output impedance. The amount of switching residue suppressed by the combined amplifier is $Z_{L1}/Z_{o,AB}$ compared to the full supply swing of D alone. So L_1 should be chosen large and AB should have low Z_o to achieve low switching ripple. However, the design of a class AB amplifier with low Z_o is quite challenging because it requires much loop-gain at high frequencies, giving rise to stability issues.

The output impedance of AB and the output inductor L_1 form a voltage divider network for the switching signal of D. The ripple voltage can be calculated by multiplying I_{thr} and $Z_{o,AB}$ (the output impedance of AB) or from $Z_{o,AB}/Z_{L1}$ with respect to the full supply swing of D alone. With a maximum switching frequency of 125MHz, the main frequency band of spurs falls outside the 2.4-2.4835GHz ISM band when the modulator is used for a IEEE 802.11g WLAN signal. The maximum allowable spurious emission in this case is -41.25dBm/MHz according to FCC 15.205 rules, which is the most restrictive in the concerned band. Since the switching frequency is varying with the envelope voltage, the peak spectral power density of the switching spurs is the most concerned parameter for emission requirements. Although it is difficult to calculate the peak spectral power density because of its dependence on the statistics of the signal, we take the pessimistic case and simplify for ripple requirements in time domain.

The output of the modulator can be expressed as the summation of the envelope signal and the switching ripple as

$$U_r(t) = A(t) + V_{rp}\cos(\omega_{rp}t) \qquad 4.23$$

Where A(t) is the time domain envelope signal and $V_{rp}\cos(\omega_{rp}t)$ is the fundamental component of the ripple at frequency ω_{rp}.

Assuming that the saturated PA has a conversion gain of 1 from its supply to its output i.e. 0dB power supply rejection, the output of the power amplifier can be expressed as

$$S_r(t) = A(t)\cos(\omega_c t + \theta(t)) + V_{rp}\cos(\omega_{rp}t)\cos(\omega_c t + \theta(t)) \qquad 4.24$$

Where $\cos(\omega_c t+\theta(t))$ is the phase modulated RF signal

Here the ripple voltage from the supply modulator is modulated with the phase-modulated RF signal, which results in a later term in equation 4.24. The resulting switching noise at the output spectrum is double sideband at the frequency $\omega_c \pm \omega_{rp}$. To have less than -41.25dBm/MHz of spurious emission for an average output power of 12dBm or -0.55dBm/MHz, the approximate ratio of the ripple voltage to average envelope voltage is

$$20\log_{10}\frac{V_{rp}}{A_{avg}} \approx -(41.25 - 0.55 - 6)dB = -34.7dB \qquad 4.25$$

Where A_{avg} is the average envelope voltage

Considering 10dB PAPR and 1dB clipping of the signal, the ratio of the ripple voltage to the peak envelope voltage, Vdd, is

$$20\log_{10}\frac{V_{rp}}{V_{dd}} = -(34.7 + 9)dB = -43.7dB \qquad 4.26$$

So, approximately -43.7dB of ripple suppression is required to have less than -41.25dBm/MHz of spurious emission for the peak output power of 21dBm. This implies that the fundamental component of the ripple should be smaller than $7.83mV_{peak}$ or $5.54mV_{rms}$ which corresponds to the output impedance of about 644mΩ at 125MHz.

4.3 Circuit Implementation of a Supply Modulator

The previous section describes the system level design choices and optimization techniques of the supply modulator for power dissipation and switching residue. This section discusses the circuit implementation. The main blocks of the supply modulator are class-AB amplifier, class-D amplifier and sense and control circuit.

4.3.1 Class AB amplifier

As discussed in section 4.2.6, AB should have a low output impedance at the switching frequency (less than 644mΩ at 125MHz) to suppress the switching noise of amplifier D which could directly affect the output PA spectrum. Also, the bandwidth of the modulator should be several times higher than the signal bandwidth to avoid distortion since the input envelope bandwidth is much higher than the signal bandwidth. To meet these very demanding requirements we used a three-stage cascoded nested Miller compensated amplifier.

Cascoded Miller Compensation

The main advantage of a cascoded Miller compensation compared to a conventional Miller compensation is explained in this sub-section. Figure 4.19(a) shows the small signal model of a well-known two stage Miller compensated amplifier. Assuming that the load capacitance (C_2) is much larger than the Miller capacitor (C_m) and that the last stage

gain $g_{m2}R_2>>1$, the small signal model results in the two-pole transfer function with the dominant pole approximately at

$$P_{1C} \cong \frac{1}{C_m R_1 g_{m2} R_2} \tag{4.27}$$

and a band limiting high frequency pole at

$$P_{2C} \cong \frac{g_{m2}}{C_2} \tag{4.28}$$

The transfer function also has a right half plane (RHP) zero.

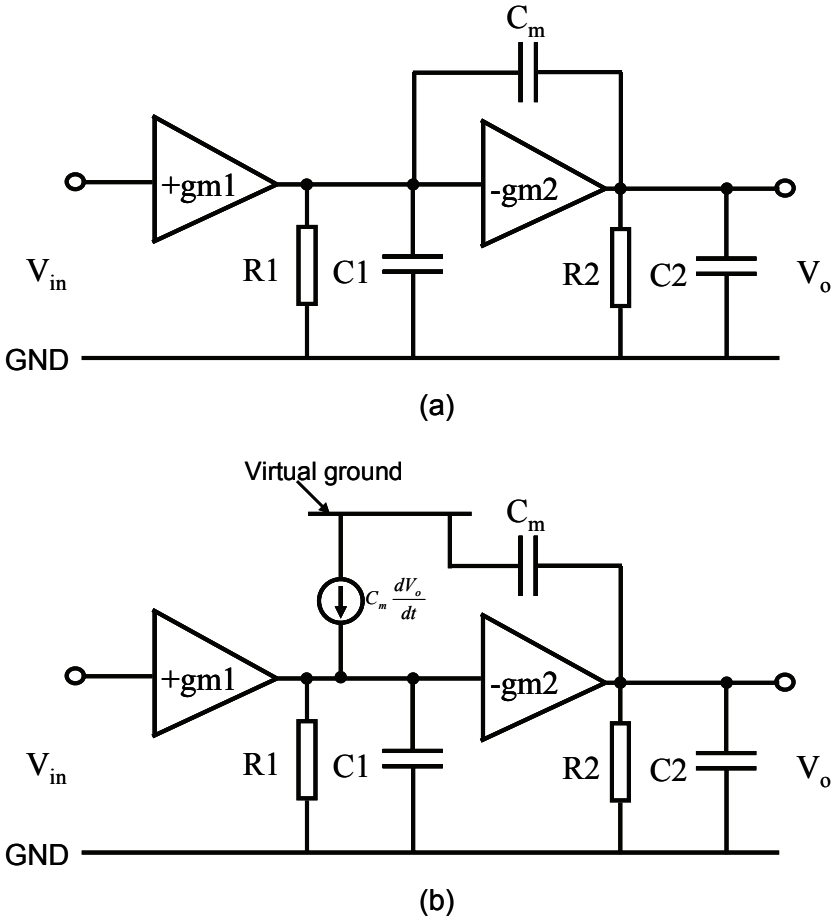


Figure 4.19 Small signal model of a two stage (a) Miller-compensated amplifier and (b) Miller-compensated amplifier with a current buffer (also called cascode configuration)

Similarly, Figure 4.19(b) shows the small signal model of a Miller compensated amplifier with an ideal current buffer. In this configuration, the compensation capacitor is shown to be connected between the output node and a virtual ground (or ac ground), while the current source charges the first stage with a copy of the capacitor current. This compensation technique is also called cascode compensation [15], [16], [17], since a current buffer with virtual ground is easily implemented in CMOS technology using a

cascode device. With an ideal current buffer, a band limiting high frequency pole is approximately given by

$$P_{2C} \cong \frac{g_{m2}}{C_2} \times \frac{C_m}{C_1} \qquad 4.29$$

So the band limiting output pole in equation 4.29, and therefore the unity-gain frequency of the cascoded Mller configuration is a factor $\frac{C_m}{C_1}$ larger than an output pole of a simple Miller compensated amplifier in equation 4.28.

Normally, the Miller capacitor is composed of the drain-gate capacitance (C_{dg}) of the output transistor(s) and an additional linear capacitor. However in case of a power amplifier with large gm in the output stage, the miller capacitor is mainly the drain-gate capacitance (C_{dg}) of the output transistor(s). In the absence of a significantly larger capacitor in parallel with C_{dg}, the cascode connection of the Miller capacitor is not so effective in a two-stage topology to increase the bandwidth. Furthermore, in our application the gain of a two stage amplifier is simply not enough anyway. To obtain very low output impedance, we implemented a three-stage nested Miller compensated amplifier.

Implementation of a Three-stage Cascoded Nested Miller Compensated Amplifier

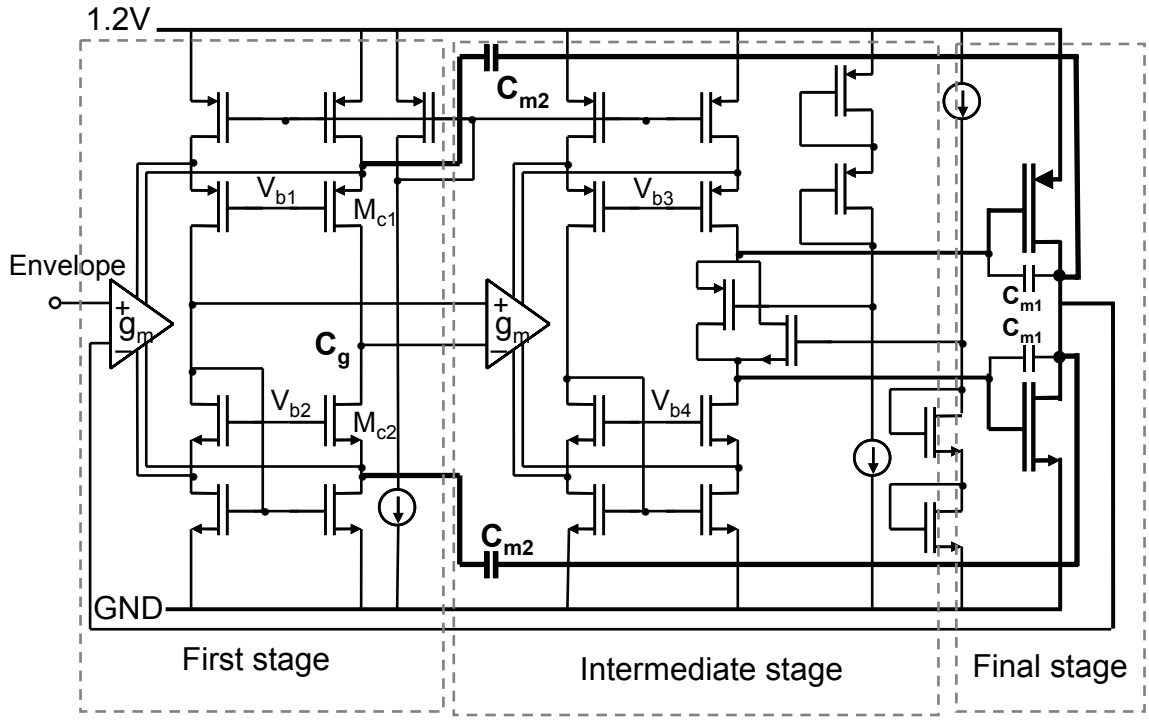


Figure 4.20 Cascoded nested miller compensated class AB amplifier

The circuit implementation of a three-stage cascoded nested miller compensated amplifier with rail-to-rail input and output as a linear amplifier AB is shown in Figure 4.20. The input stage was designed to have rail-to-rail input and output swing. A folded cascode configuration with complementary NMOS and PMOS input pairs are used such that when the input reaches to one of the supply rail, one of the pair stays active. These input pairs are loaded with folded cascodes instead of current mirrors to ensure rail to rail output. When common mode of the input is at mid-supply, the total transconductance of the input stage is twice that of either the NMOS or the PMOS pair alone. Thus, the input transconductance is subject to 2:1 swings over the course of normal operation. Though several techniques are proposed in the literature to make this gm constant, for our application it is not necessary to compensate because it will just result in two times variation in output resistance which is tolerable. The intermediate stage is similar to the input stage and has a rail-to-rail input/output capability. The floating current source at the output of this stage is used to set the Quiescent-point for the class AB output stage. An inverter configuration is used for the output stage in order to have rail to rail output.

The inner amplifier is compensated with simple miller compensation through C_{m1} whereas the outer feedback loop is compensated through an outer miller capacitor C_{m2}. The cascode compensation is obtained by connecting the outer miller capacitor C_{m2} to the source of the cascode transistors (M_{c1}, M_{c2}) of the first stage [15] resulting in the cascoded nested-Miller compensated amplifier. With cascoded miller, the cascode transistors (M_{c1}, M_{c2}) buffer the miller capacitor current and feed this current into equivalent capacitor (C_g) at the gain node, which converts it back to a voltage. So when $C_{m2}>C_g$, the maximum feedback factor can be larger (than 1) by a factor C_{m2}/C_g. This in turn shifts the output pole of the cascoded Miller compensated amplifier to a frequency which is a factor C_{m2}/C_g larger than the output pole of an amplifier with simple miller compensation as discussed in the above sub-section. This permits a higher unity gain frequency and decreases the output impedance of the amplifier. The resulting amplifier has a unity gain frequency of 340MHz with 5.3Ω||2pF load, which is almost 3 times higher than a simple nested miller compensated amplifier with the same power consumption. The simulated output impedance of the class AB amplifier is about 0.42Ω at 125MHz which is within our requirement. The cascoded miller loop also introduces a second non-dominant pole which occurs due to the finite source impedance of the cascode transistor. However this pole can be placed far from the unity gain frequency to avoid stability problems.

4.3.2 Class D amplifier

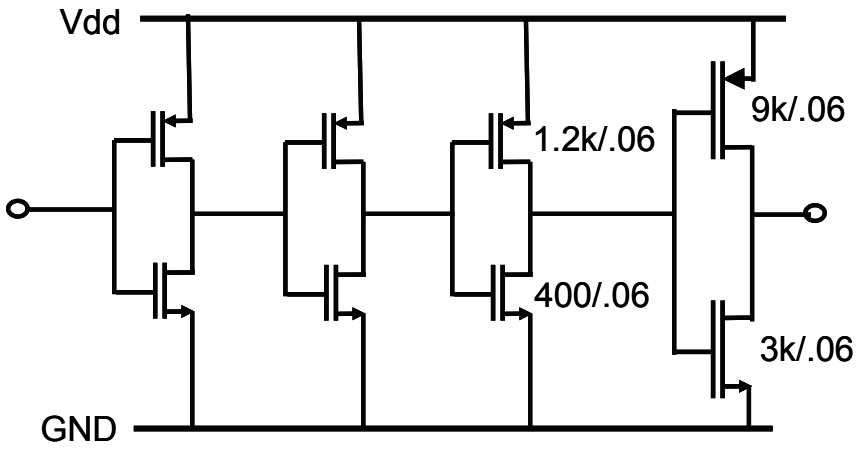


Figure 4.21 Class D amplifier

The class D amplifier is simply a chain of inverters as shown in Figure 4.21. The conduction loss of the output stage is,

$$P_{con} = I^2 R_{eq} = I^2 [D.R_{dsP} + (1-D)R_{dsN}] \quad 4.30$$

where R_{dsP} and R_{dsN} are the switch resistance of PMOS and NMOS respectively and D is the duty cycle.

The switching loss of the output stage is,

$$P_{sw} = C_{eq} f V_{dd}^2 \quad 4.31$$

Here, C_{eq} represents the total equivalent capacitances of the output stage that contributes to the switching loss. C_{eq} is proportional while R_{eq} is inversely proportional to the area of the output transistors which have the same length. Considering main losses are in the conduction and switchings, the optimum area that minimizes $P_{con}+P_{sw}$ can be found by setting the first derivative to zero. This leads to equation 4.18 for the optimized area. This way, the sum of switching and conduction loss is minimized by proper dimensioning of the NMOS and PMOS transistors for 90mA of output current, leading to W/L of 9k/0.06 (PMOS) and 3k/0.06 (NMOS) for the power transistors at a switching frequency of 100MHz. This optimization was done at the 6dB back-off power level (at $V_o=V_{dd}/2$ i.e. $\alpha=0.5$). The reason is as follows. The WLAN OFDM signal has the highest probability density in the region of ~0.5 to 3.5dB above the average power (see Figure 4.13). So, at ~8dB below the peak power (i.e ~3.5dB above the average power), the probability density is still comparable. Obviously, efficiency matters most at high power and high probability density region, so in the later case. Moreover in practice, it is possible to clip 1-2dB while still satisfying the linearity requirements. So we choose to optimize at 6dB below peak power i.e. at $V_o=V_{dd}/2$.

The size of the driver is chosen such that the total loss in the power and driver stage is minimized. The driver transistors are 7.5 times smaller.

4.3.3 Sense and control circuit

Figure 4.22 shows the current sense and control circuit consisting of a hysteretic comparator. Main function of this circuit is to measure the current supplied by AB and generate a control signal with hysteresis for D. The control signal should be as follows: when the current supplied by AB exceeds an upper threshold current level I_{thrH}, D should be turned 'on'. Similarly when the current supplied by AB reaches a lower threshold current I_{thrL}, D should be turned 'off'. By choosing $I_{thrL}=0$ and $I_{thrH}=2I_{thr}$, we make sure that the sensing of only positive output current of AB by the sense and control circuit is enough. Although the output current of AB could be negative, it is not needed to be sensed.

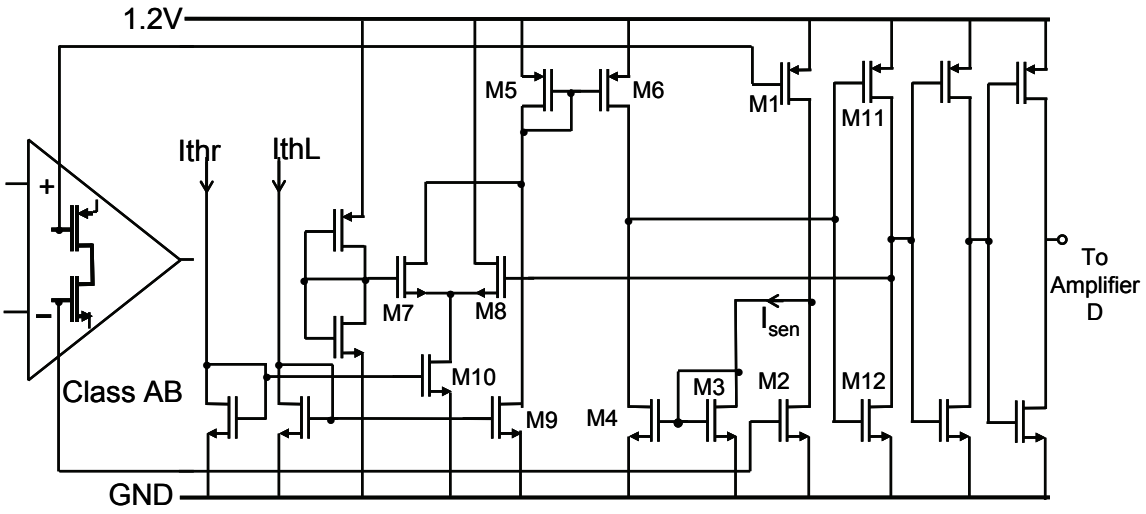


Figure 4.22 Sense and control circuit

The circuit in Figure 4.22 is based on the current comparison through simple current mirrors. Scaled copies of the current of the output transistors of AB are made via M1 and M2 and the difference current (I_{sen}), which is proportional to the output current of AB, is flowing through M3. The currents through M3 and M5 are compared via its matched pairs M4 and M6. Current through M5 depends upon the threshold levels. The output of M4 and M6 drives an inverter (M11 and M12) and also controls the differential switching stage (M7 and M8) via this inverter providing a regenerative feedback loop. The hysteresis current of the sensing circuit is set by I_{thr} and the lower threshold current is set by I_{thL}. One disadvantage of this sense and control circuit is its inability to sense the output current of AB accurately when the output transistor of AB enters its linear region. This results in a shift of threshold current of the sensing circuit while AB is out of saturation. However, this threshold current shift is mostly compensated by the reduction in switching frequency caused by being close to the supply rails. It will not increase the power dissipation of AB significantly.

4.4 Circuit Implementation of a Class-E RF Power Amplifier

The features of class-E Power Amplifier such as the simplicity of matching network, and the zero-voltage switching even at very high frequency makes it the best candidate for the integrated polar modulated power amplifier system for WLAN. The operation of class-E power amplifier is discussed in chapter 2. The circuit composition and design issues are discussed in this section.

Basic Class-E Circuit

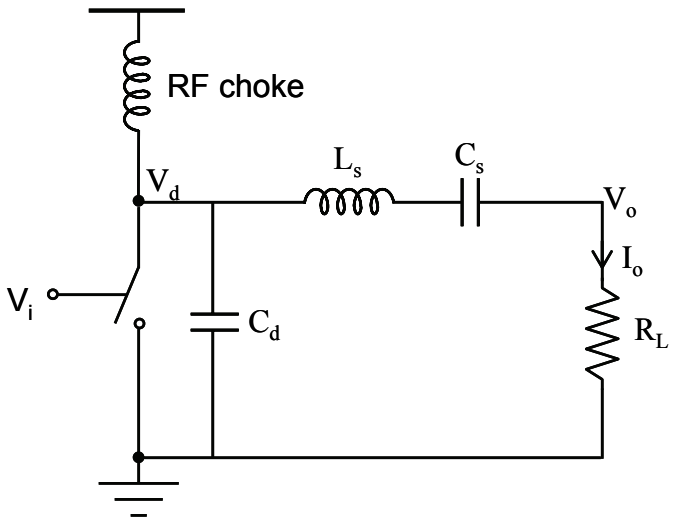


Figure 4.23 Simplified circuit of a class-E power amplifier

Figure 4.23 shows the basic class E power amplifier. The component values: optimal load resistance (R_L), the shunt capacitor (C_d), the series inductance (L_s) and the series capacitance (L_s) are the function of supply voltage (V_{dde}), output power (P_{out}), loaded quality factor (Q) and operating frequency ($\omega=2\pi f$). The following design equations, derived in [18], can be used to calculate the component values

$$R_L = \frac{8V_{dde}^2}{P_{out}(4+\pi^2)} \tag{4.32}$$

$$L_s = \frac{QR_L}{\omega} \tag{4.33}$$

$$C_d = \frac{1}{5.447\omega R_L} \tag{4.34}$$

$$C_s = C_d\left(\frac{5.447}{Q}\right)\left(1+\frac{1.42}{Q-2.08}\right) \qquad 4.35$$

The above design formulas are based on the following assumptions

- the switch-on resistance is negligible
- the drain efficiency is 100%
- the inductance of the RF choke is very high
- the switch duty cycle is 50%

Note that the supply voltage (V_{dde}) is same as the modulator output voltage (V_o) of section 4.2

Differential Class-E circuit

To have the measurement flexibility in our test chip we prefer to use bond-wires instead of flip-chip to connect the chip to the outside world. When the bond-wires are used for ground connections, the single ended PA configuration can take up large voltage headroom and may even possess stability problems due to its large inductance values (~1nH/mm). A simple solution is to use multiple bond-wires. However this cost extra bond-pads. Furthermore because of mutual coupling, the decrease in inductance is not directly proportional. So a differential topology is used. The advantage is that the ac current circulates inside the chip, so the ground terminal inside the chip acts as a virtual ground. This alleviates the substrate coupling problem and also helps to boost the gain [19]

Output Matching

An output matching network is usually needed to transform the antenna impedance or the input impedance of the balun to the optimum load resistance (R_L) of the amplifier. The simplest and easiest matching network for practical implementation is the L-type network as shown in Figure 4.24. The network requires only an inductor and a capacitor.

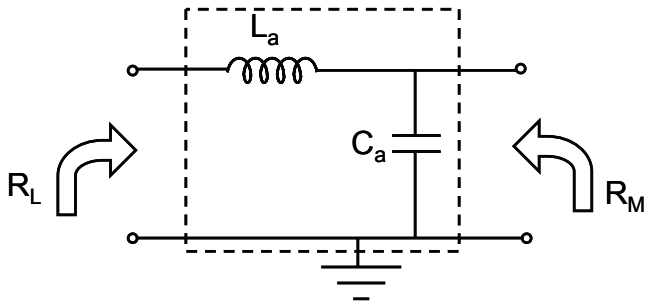


Figure 4.24 L-type match network

The loaded quality factor, which is defined as the ratio of the resonance frequency to the 3-dB bandwidth, of the L-type matching network is given by [20],

$$Q_L = \sqrt{\frac{R_M}{R_L} - 1} \tag{4.36}$$

The matching circuit parameters can be calculated from equations below [20],

$$C_a = \frac{Q_L}{\omega R_M} \tag{4.37}$$

$$L_b = \frac{Q_L R_L}{\omega} \tag{4.38}$$

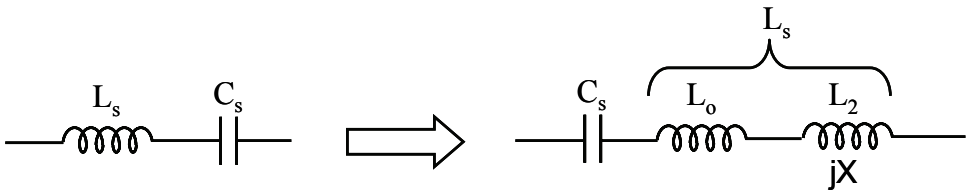


Figure 4.25 Rearrangement of network elements

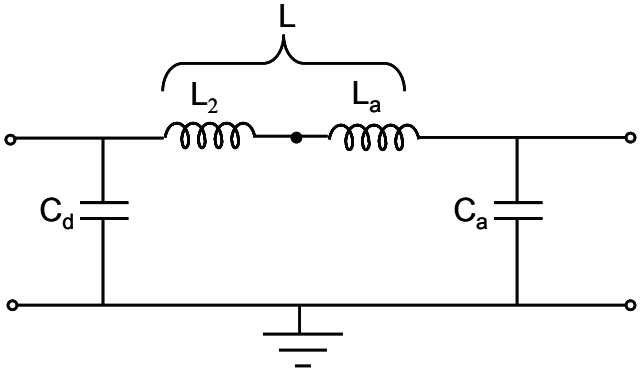


Figure 4.26 Rearrangement of matching network after removing the tank (C_sL_o)

The series resonant circuit elements L_s and C_s of the class-E amplifier in Figure 4.23 can be rearranged as shown in Figure 4.25. The tank (C_sL_o) forms the resonating network at the operating frequency such that $\omega = \frac{1}{\sqrt{L_o C_s}}$. The L-type output matching of Figure 4.24 also forms the resonating network from L_a and C_a. In practical RF circuit implementation the resonating network L_o and C_s can be removed from the circuit while still satisfying the class-E conditions due to the presence of L_a and C_a [20] as a resonating tank (see Figure 4.26). The benefit is that the circuit performance will be dependent on fewer components as one tank circuit is removed. However the dc-blocking capacitor is still needed. L_2 in Figure 4.26 can be calculated as

$$L_2 = L_s - \frac{1}{\omega^2 C_s} = \frac{QR_L}{\omega} - \frac{1}{\omega^2\left(C_d\left(\frac{5.447}{Q}\right)\left(1+\frac{1.42}{Q-2.08}\right)\right)} \quad 4.39$$

Balun

A Lattice type LC-balun is used for converting the differential PA output into a single ended signal. The lattice-type balun is attractive because of its compactness. It is based on lumped components and consists of two inductors and two capacitors as shown in Figure 4.27, which produce the ±90° phase shift. R_i is the balanced input impedance of the balun. That means each input side will see $R_i/2$ impedance. Ro is the load impedance which is usually antenna impedance. The circuit parameters can be calculated by [21],

$$L_b = \frac{Z_c}{\omega} \quad 4.40$$

$$C_b = \frac{1}{\omega Z_c} \quad 4.41$$

Where $Z_c = \sqrt{R_i R_o}$

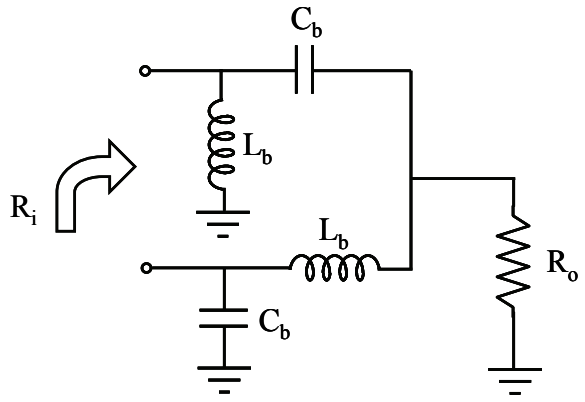


Figure 4.27 Lattice type LC-balun

Output Stage Circuit Design

Figure 4.28 shows the complete output-stage of the class-E power amplifier. The series resonance circuit L_0C_s is not present as discussed above. So the inductor $L=L_a+L_2$. The targeted output power (Pout) is 220mW at V_{dde}=1.2V with an assumption of 100% drain efficiency. The supply modulator is optimized to supply about the same output power at the output voltage of 1.2V (recall section 4.2.5, I=90mA for α=0.5). However, in practice the output voltage of the modulator can not reach 1.2V because of the voltage drop across the switch.

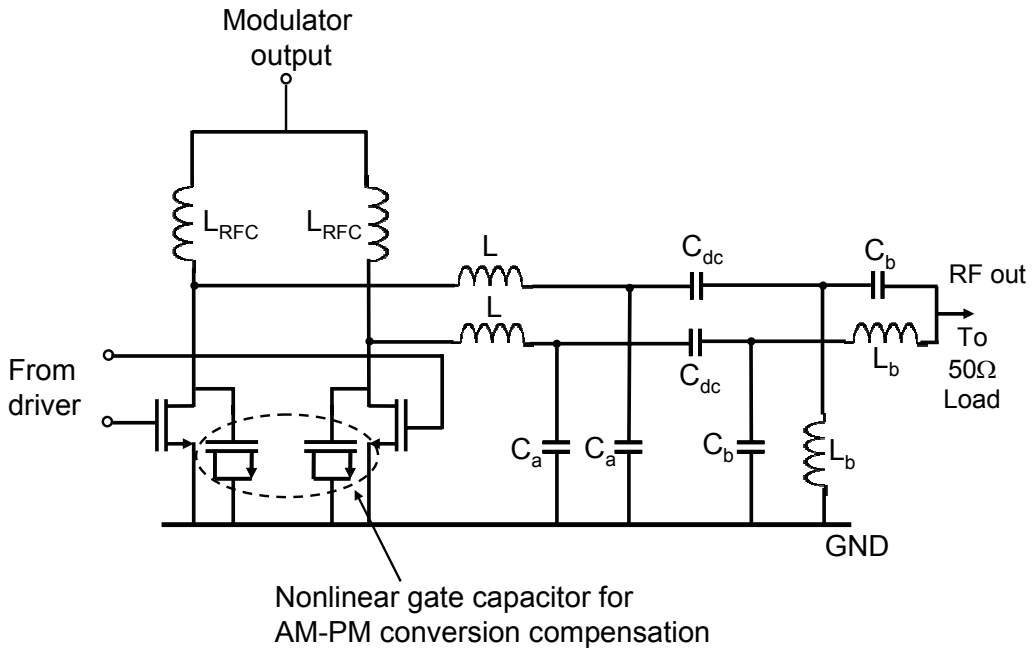


Figure 4.28 Differential class-E power amplifier

The targeted P_{out} for each amplifier of the differential pair is 110mW. The operating frequency, f=2.41GHz. Choosing the loaded quality factor, $Q=Q_L=7$, the load network values calculated from equations 4.32-4.41 are $R_L=7.5\Omega$, L_s= 3.5nH, C_d=1.6pF and C_s=1.6pF. The matching network parameters are L_a=1.18nH, C_a=3.1pF and the circuit parameters for balun are L_b=4.7nH and C_b=0.93pF. Furthermore $L=L_a+L_2$=1.96nH.

Simulation was done in the Spectre circuit simulator with a real transistor model to fine tune the circuit components values. With a switch transistor size of 3.5k/0.28, the received component parameters are L=1.55nH, C_a=3.8pF, L_b=4.7nH and C_b=0.94pF. The shunt capacitance C_d is composed of the MOSCAP and the drain-source capacitance of the output transistor. The size of the transistor used as MOSCAP is 800/0.28. C_{dc} and L_{RFC} are chosen 10pF and 8nH respectively. The simulated drain efficiency is 87.2%. The dc-current drawn from the supply is 184mA. Thick oxide transistors are used in the class E PA design -including the MOSCAPs- to handle the large swing at the drain of the transistors.

Driver circuit

In our application, the power amplifier works in large power back-off most of the time. However the dissipation in driver remains same regardless of back-off. The 2-stage regenerative driver that saves the drive power is shown in the Figure 4.29. The driver stage also consists of the RLC network (resonant tank). The energy stored in the gate capacitance of the power transistor is transferred back and fourth to the RLC network to reduce the dissipation. The Q-value of the resonant tank should be low enough to ensure that the phase information is preserved. It should also be high enough to save the maximum drive power.

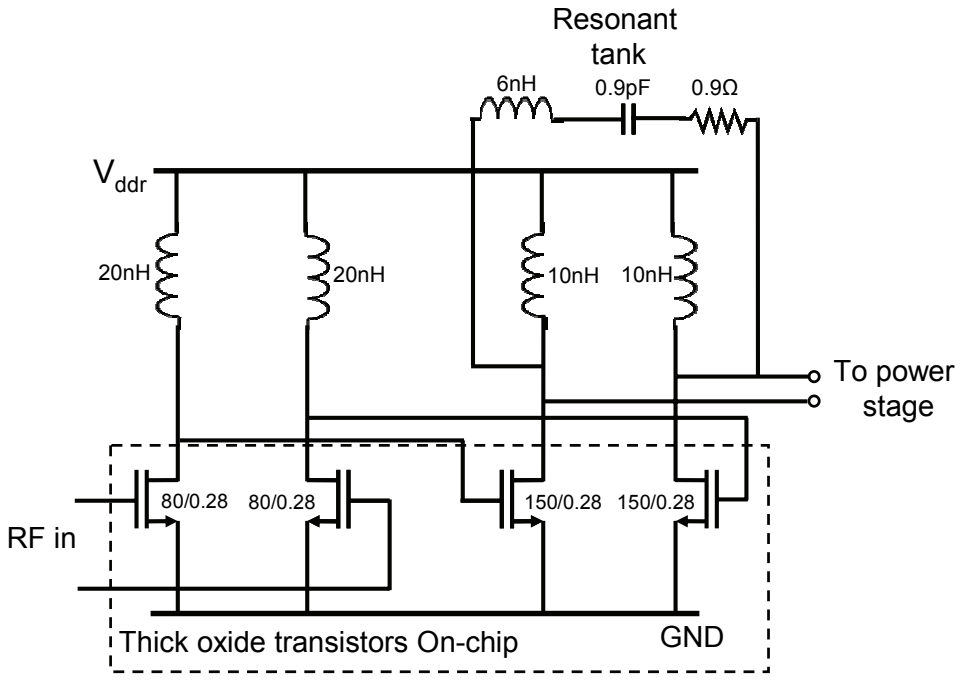


Figure 4.29 Resonant driver

AM-PM Compensation

The class E power amplifier is also partially compensated for AM-PM conversion. As discussed in sub-section 4.1.5 one source of AM-PM distortion in Class E PA's is the nonlinear drain-bulk junction capacitance of the output transistor. As the supply voltage is reduced the drain bulk capacitance (C_{db}) will increase which causes the phase of the output RF signal to change. We used a simple way to partially compensate this distortion by replacing the shunt capacitor of the class E PA across the drain-source with a nonlinear gate capacitor or MOSCAPs (C_{gs}) as shown in Figure 4.28. As opposed to C_{db}, C_{gs} decreases with the supply voltage. The width of the transistor can be chosen such that the combination works more as a linear capacitor for a large part of the supply voltage range, at the same time satisfying the zero voltage switching (ZVS) condition needed for the class E amplifier.

To illustrate the effect of compensation we take the design example of the power amplifier from sub-section 4.1.5. The parallel capacitor (C_d) in the design is composed of the linear capacitor of 1.4pF and the nonlinear drain-bulk capacitor modeled by equation 4.7 with C_{jo}=1.7pF, m=0.5 and V_{bi}=0.71V. Now, we replace the linear capacitor with the MOSCAP of the size 820/0.28. The phase variation of the output signal with the linear capacitor and with the compensation using MOSCAP is shown in Figure 4.30. It is clear from the figure that the compensation with MOSCAP improves the AM-PM distortion. The nonlinear drain-source capacitance and the MOSCAP values as a function of the supply voltage are shown in Figure 4.31.

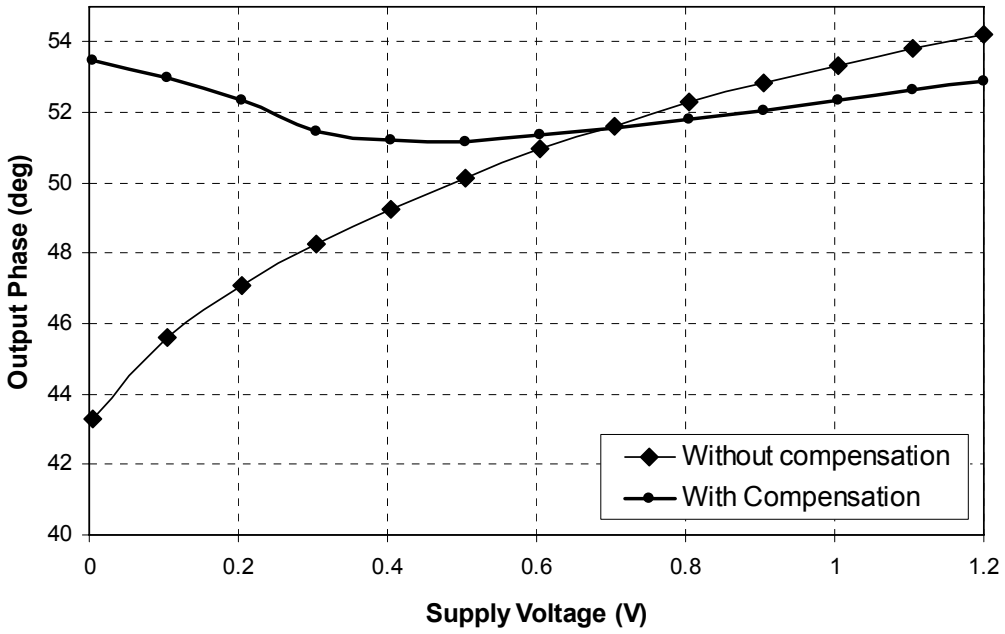


Figure 4.30 Output phase of the power amplifier, shown in the design example of sub-section 4.1.5, with the MOSCAP compensation and without compensation (using the linear capacitor). The output transistor is an ideal switch but with the non-linear drain-bulk capacitance modeled using equation 4.7.

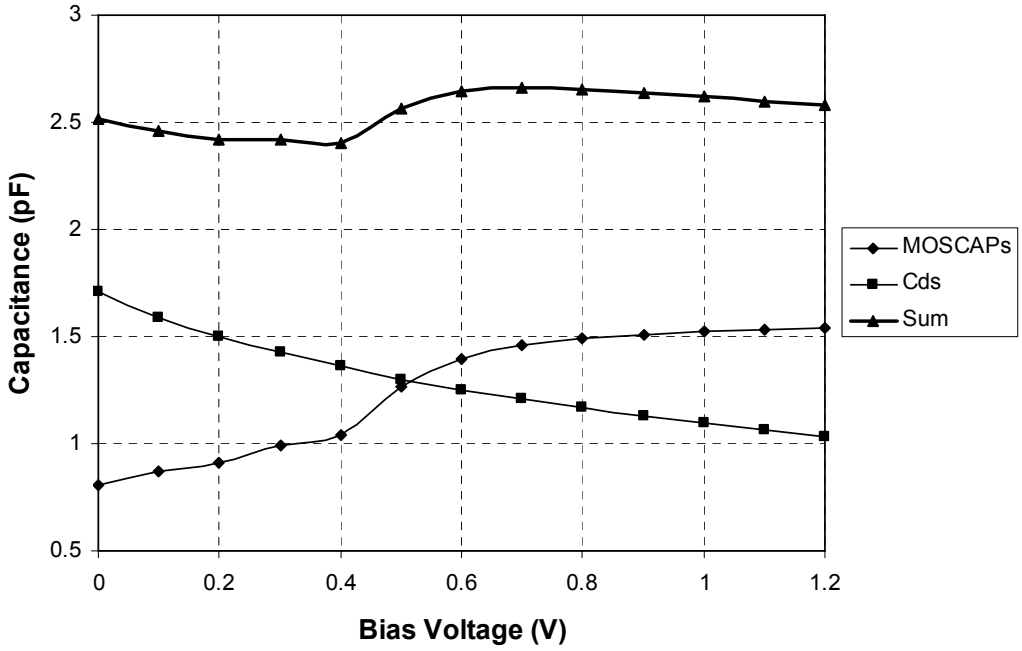


Figure 4.31 Nonlinear drain-bulk (source) capacitance with C_{jo}=1.7pF, m=0.5 and V_{bi}=0.71V and capacitance of the MOSCAP of the size 820/0.28

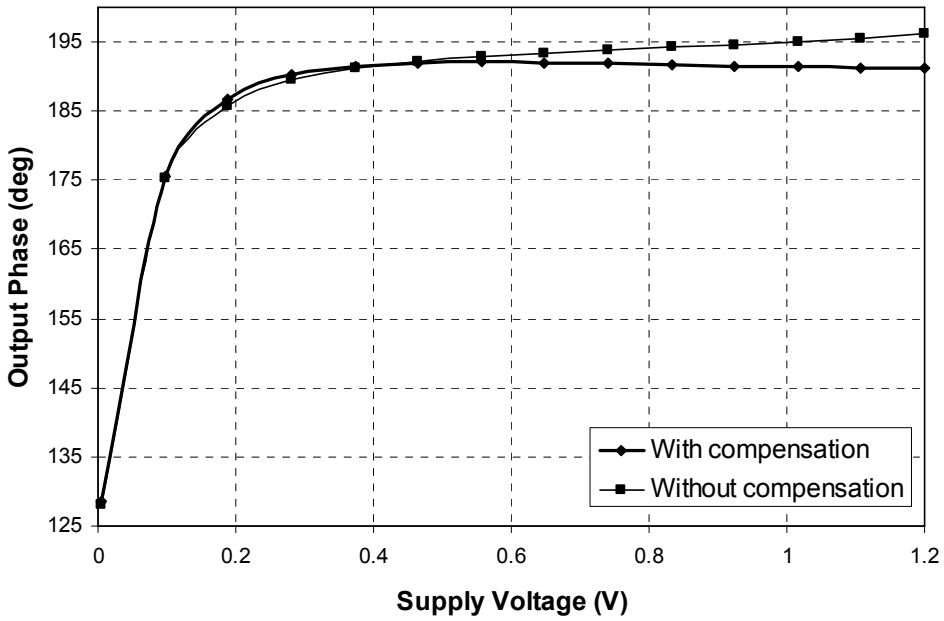


Figure 4.32 AM-PM conversion of the power amplifier of Figure 4.28 with and without compensation. The switches of the PA are CMOS transistors of size 3.5k/0.28. The AM-PM conversion is both due to the nonlinear drain-bulk capacitance and the feed-through via the parasitic drain-gate capacitance.

Figure 4.32 shows the AM-PM conversion of the implemented differential Class-E circuit of Figure 4.28 with the linear capacitor of 1.2pF and with MOSCAPs of 800/0.28. The improvement is visible for the large part of the supply voltage range (0.3V to 1.2V). The AM-PM conversion in Figure 4.32 is both due to the feed-through and the nonlinear drain-bulk capacitance. The compensation also helps to reduce the AM-PM distortion due to feed-through, since the phase change in this case is also opposite. However for small Vdd (<0.3V), the phase distortion mainly due to feed-through is significant. Although only partial compensation of AM-PM conversion is possible with this technique, it does not require any extra circuitry. Furthermore, C_{db} and C_{gs} have very different characteristics over process, voltage and temperature variations. So the reduction in AM-PM distortion is limited.

RF Choke

The value of the RF choke ('L_{RFC}' in Figure 4.28) is extremely important for the supply modulated PA, unlike for fixed supply PA's. L_{RFC} should be high enough for RF isolation and low enough to provide sufficient bandwidth for the supply modulation as the envelope bandwidth is high. The RF choke of 8nH is chosen to satisfy these requirements. Band limitation by L_{RFC} could directly influence the linearity of the whole PA system.

4.5 Measurements

4.5.1 Polar Modulated Power Amplifier Module Prototype

The demonstrator chip was fabricated in a 65nm CMOS process. Figure 4.33 shows the chip micrograph with a total chip area of 1.1×1.2mm^2. The active area of the modulator is 0.1043mm^2. The chip contains the supply modulator and the class-E PA of a polar modulated system.

The die, the output matching network, the LC balun and other passive components are placed on a laminate module to enable a fully integrated polar modulated amplifier system. The laminate technology allows integration of surface mount components and multiple dies in a single package in an inexpensive and reliable way. Laminate modules also provide a foundation for stacked-die and flip-chip technology. However, in our application the die is wire-bonded to the laminate for measurement flexibility. Some small inductors are made in a laminate substrate itself.

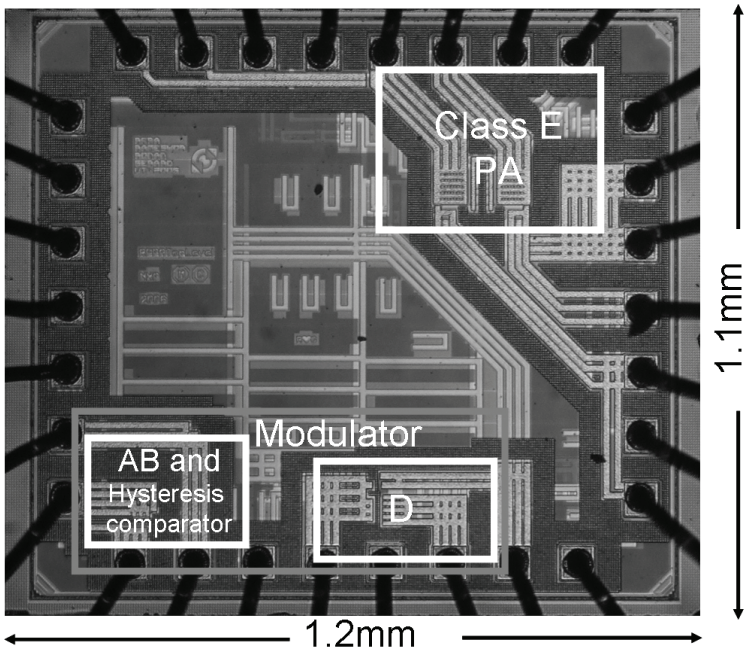


Figure 4.33 Micrograph of the chip

The LAMP3 variant of the laminate technology is used in our application. The schematic cross-section of the laminate substrate is shown in Figure 4.34. The LAMP3 has 4-metal layers. The top and the bottom metal layers have thickness of 25um and the inner metal layers have a thickness of 22um. The dielectric layer-1 and -3 as shown in Figure 4.34 are 40um thick where as the layer-2 is 250um thick.

The fabricated laminate module with an area of 4×8mm^2 is shown in Figure 4.35. The area is not fully optimized. This is because we have chosen the standard size of laminate

that fits to the available test board (PCB) to save design time for the test board. Figure 4.36 shows the backside view of the laminate module. The backside is connected to the test board for the measurement.

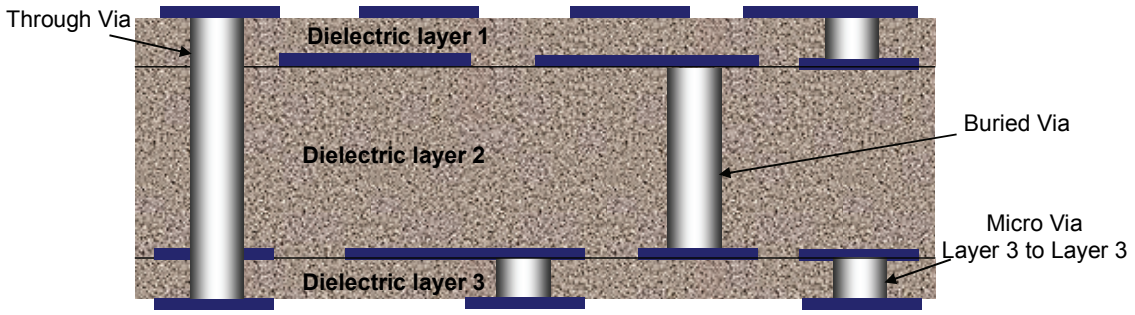


Figure 4.34 Schematic cross-section of the laminate substrate

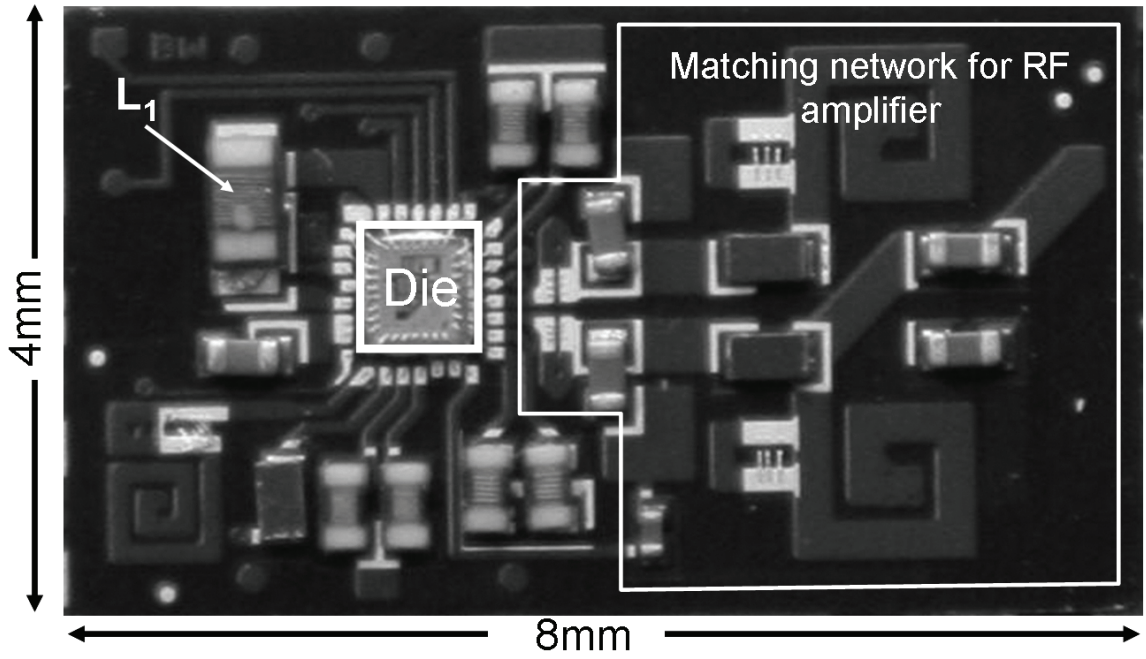


Figure 4.35 Demonstrator chip on laminate module

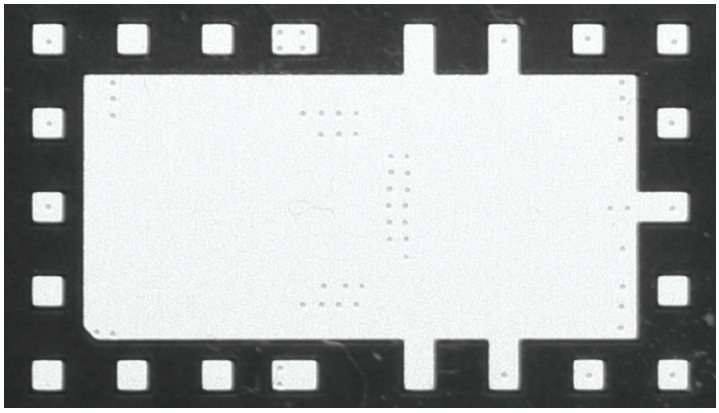


Figure 4.36 Backside view of the laminate module

4.5.2 Measurement Setup

Figure 4.37 shows the block diagram of the measurement setup that was used to test the polar modulated power amplifier module. The amplitude and phase signals of the IEEE 802.11g 64QAM OFDM WLAN have to be provided as inputs to the test chip. The WLAN test signal from the WLAN design library of the Advanced Design System (ADS) software is used for this purpose. The signal is decomposed into amplitude and phase in ADS. The amplitude and phase signal are then downloaded to two vector signal generators (E4438C and E8267D) from Agilent. The signal generators are synchronized to align the symbol timing between the two signals by using a built-in frequency reference. The vector signal generators then generate the phase modulated RF signal and the amplitude signal. The RF signal is made differential by using a balun, which is a M/A-COM H-183-4, 30-3000MHz.

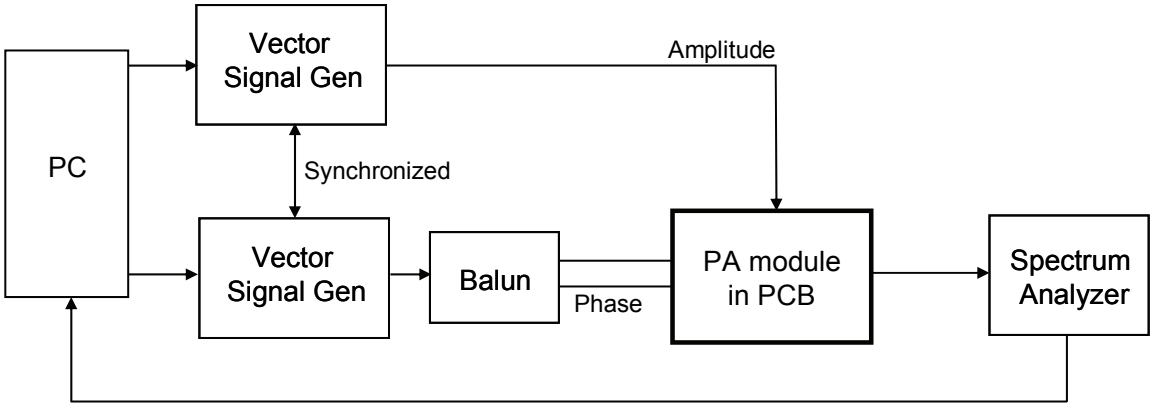


Figure 4.37 Block diagram of experimental setup

The output signal of the power amplifier is connected to the Agilent PSA spectrum analyzer (E4440A) for measurement. The output spectrum is measured in the spectrum analyzer. However, to measure EVM and to plot the constellation of the incoming signal, the Agilent 89600 Series Vector Signal Analysis (VSA) Software is used in the PC. The

VSA software takes the real-time down-converted data from the spectrum analyzer to characterize the incoming signal.

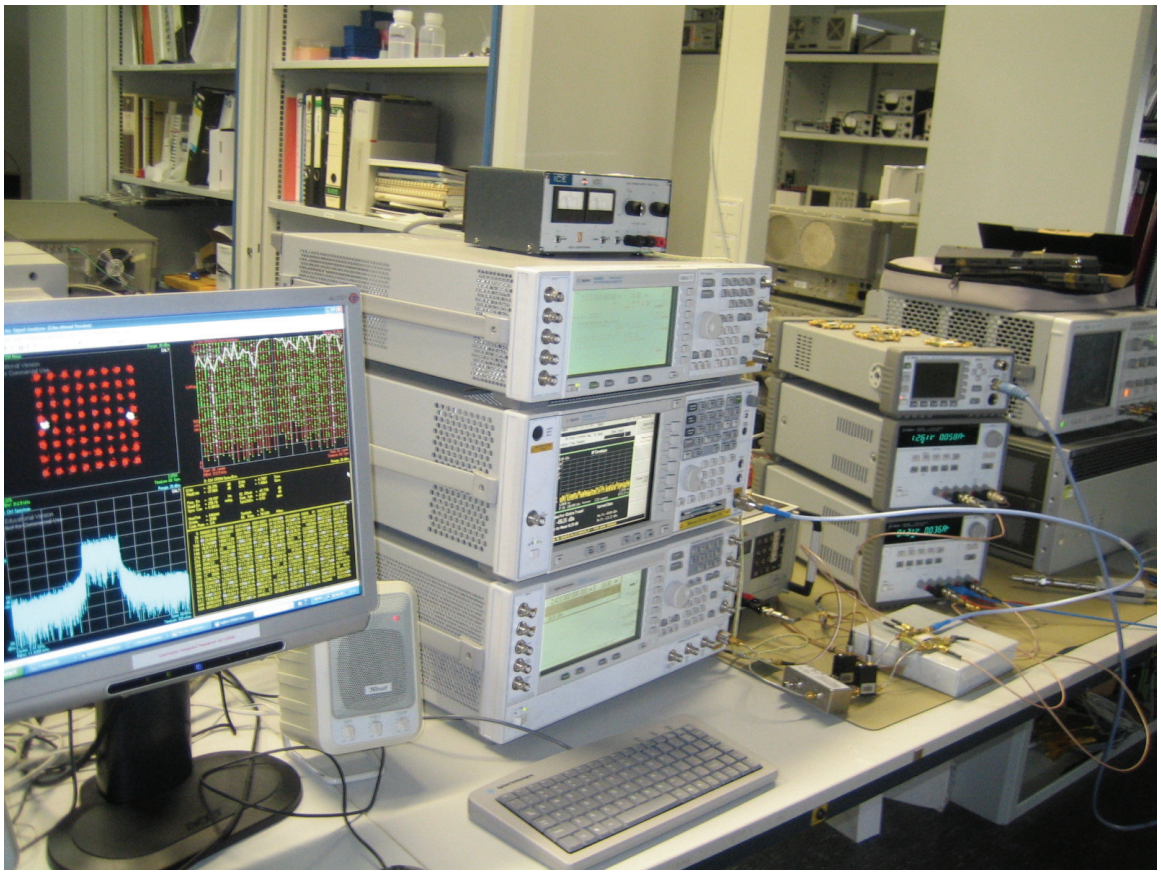


Figure 4.38 Lab experimental setup

An Agilent 86100A Digital Communication Analyzer is used to capture the time domain signal such as the output signal (envelope) of the modulator. Similarly, an HP 4195A Impedance/Network Analyzer is used to measure the output impedance of the class-AB amplifier. A photograph of the lab setup is shown in Figure 4.38.

4.5.3 Measurement Results

The output inductor L_1 of the modulator in Figure 4.35 is 80nH (SMD 0603), off-chip. Figure 4.39 shows the measured DC efficiency performance of the supply modulator with respect to its output power with a supply voltage of 1.2V and a 5.3Ω load instead of a class E PA. It delivers a 22.7dBm of peak output power with a peak efficiency of 87.5%. The efficiency stays above 40% with 10dB of output power back-off. When compared to the measured efficiency of the stand-alone AB amplifier for the same 10dB of output power back-off, the presented modulator shows an efficiency that is almost double as high. The non-monotonic increase in efficiency curve at high output power (21.8dBm and higher) is because the class D amplifier stops switching. This prevents switching loss and hence the efficiency increases.

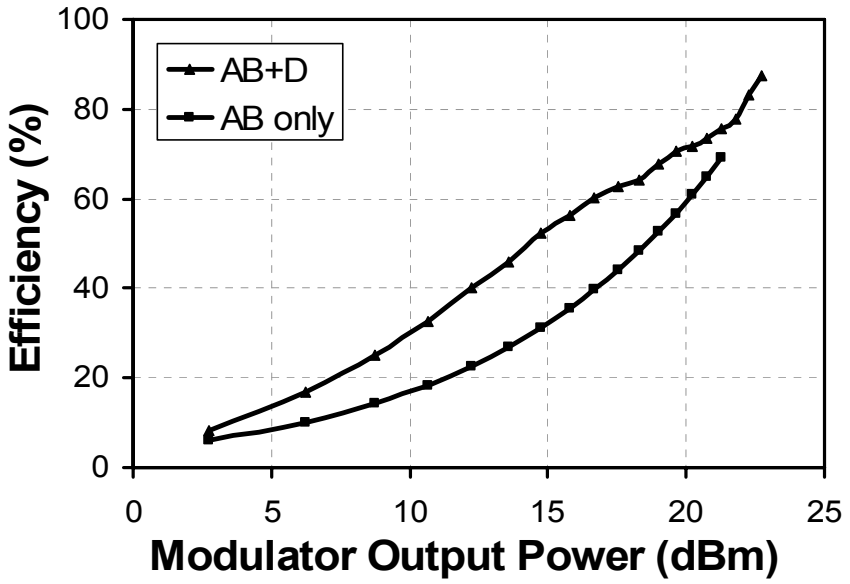


Figure 4.39 Measured Efficiency performance of the supply modulator

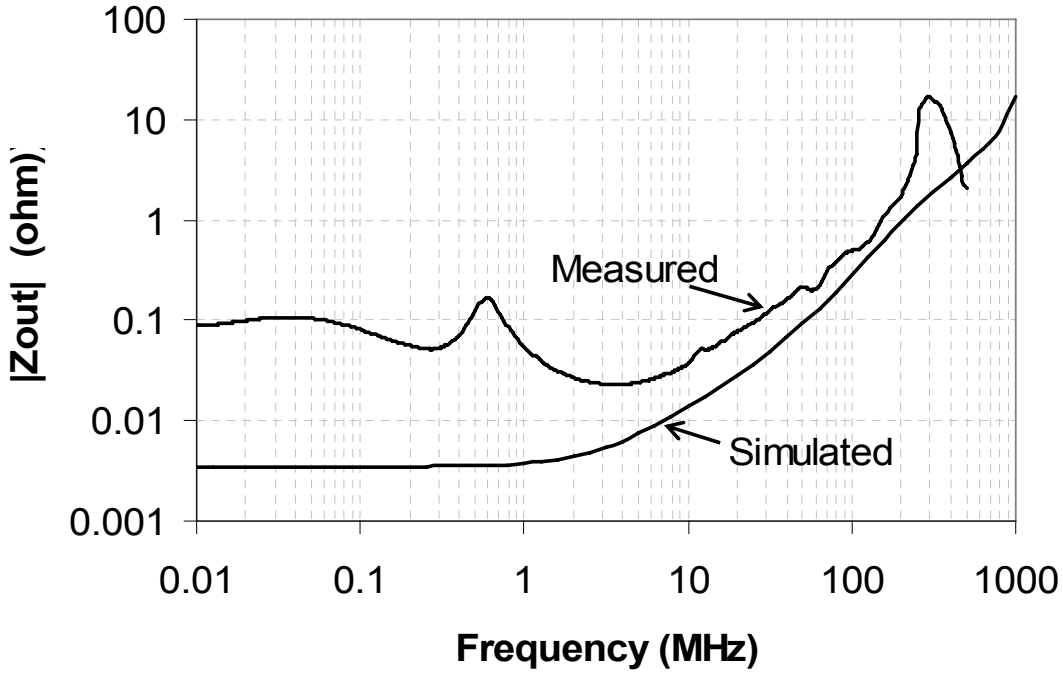


Figure 4.40 Measured and simulated output impedance of AB at V_o=0.6V

Figure 4.40 shows the measured and simulated output impedance of the amplifier AB at V_o=0.6V The measured output impedance is below 0.21Ω up to 50MHz frequency. At 100MHz the output impedance is 0.5Ω. Figure 4.41(a) shows the switching voltage ripple

for a dc input voltage. The switching ripple is 4.3mVrms at the switching frequency of 118MHz, which meets our requirement of less than 5.54mV$_{rms}$.

The amplitude of a IEEE 802.11g WLAN signal is applied to the modulator with a 5.3Ω load. Figure 4.41(b) shows the superimposed input and output waveforms. The measured small signal (-3dB) bandwidth of the modulator is 285MHz and the power bandwidth, the bandwidth over which an amplifier can deliver at least half of its maximum output power, is 45MHz.

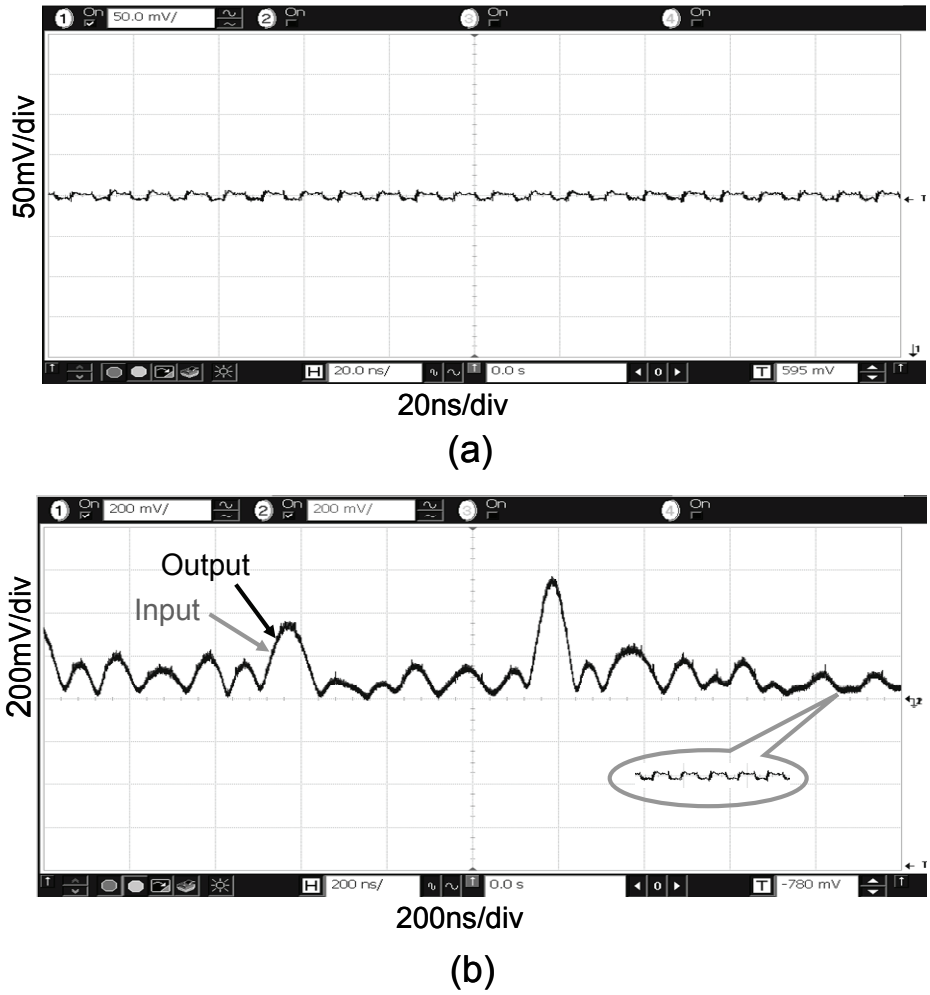


Figure 4.41 a) Time domain waveform showing the switching ripple b) Superimposed input and output waveforms of the modulator for the amplitude of the IEEE 802.11g WLAN signal.

These measurements suggest that the modulator is good enough to use for WLAN purposes. Two synchronized vector signal generators were used to generate amplitude and phase of the IEEE 802.11g WLAN OFDM signal with random data and to convert the phase signal to the desired RF output as discussed in sub-section 4.5.2. The static time misalignment between the amplitude and the phase path is adjusted through software.

Figure 4.42(a) shows the measured output spectrum. We see that the spectral mask is satisfied. Figure 4.42 (b) shows the constellation. The measured EVM is -26.1 dB for 54Mbps data rate. Figure 4.43 shows the output spectrum for a larger frequency band of 1.5GHz. This figure mainly shows the switching noise at the output spectrum. The switching noise is less than -42.5dBm/MHz at full output power, satisfying the FCC, ETSI and ARIB rules for spurious emissions.

Operating at 2.41GHz, the polar modulated PA system delivers an average output power of 11.75dBm with an average PAE of 13.1% for the WLAN signal, including all losses in the passive components of the matching network and balun. Although the efficiency is much higher compared to a class A linear amplifier (3.81% in [22]), it is lower than expected. Measurements show that the stand-alone class E amplifier efficiency is only 21.7% for the OFDM signal due to excessive bond-wire inductance at the outputs of the differential class-E amplifiers. This is because the wafer that we received was not grinded to thin-down the die, which resulted in a longer bond-wire than expected. Since the bond-wire inductance is part of the resonating network of the class-E PA in our implementation, its larger value reduces the output power and hence the efficiency. Based on simulations and literature [23], there should be ample room to improve the class E efficiency.

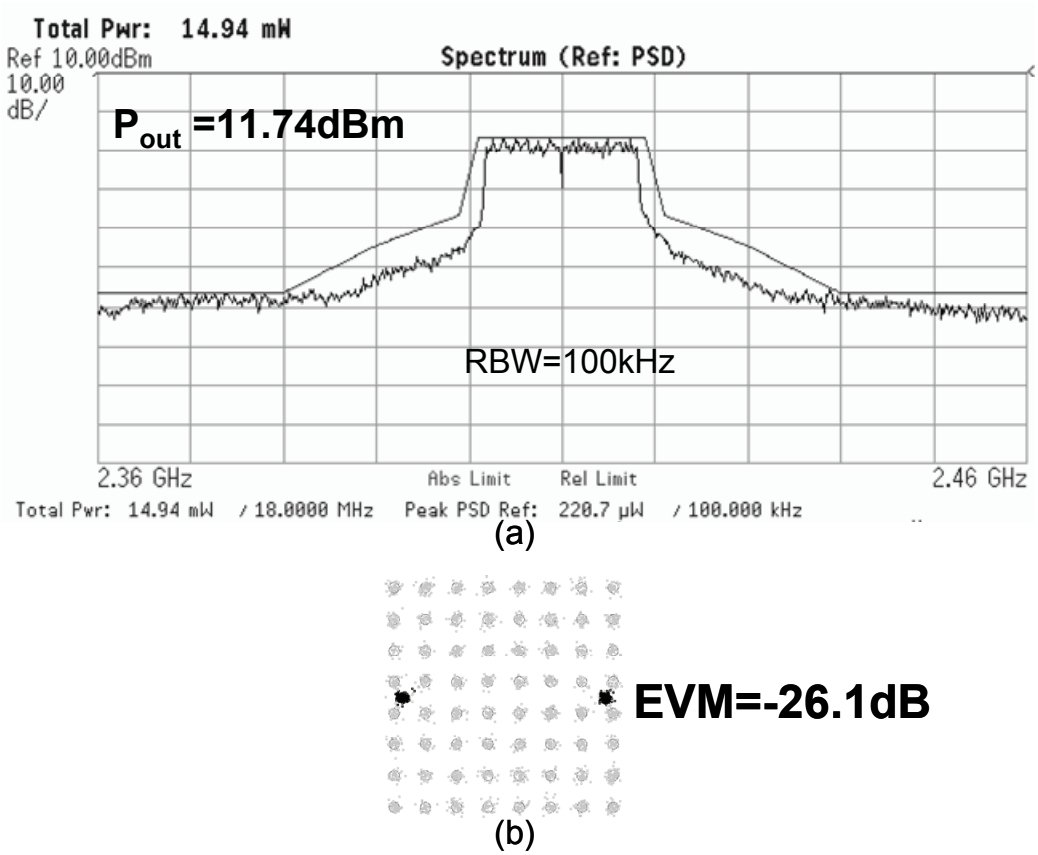


Figure 4.42 Measured (a) output spectrum of the modulator with class E PA and (b) constellation with IEEE 802.11g spectral mask

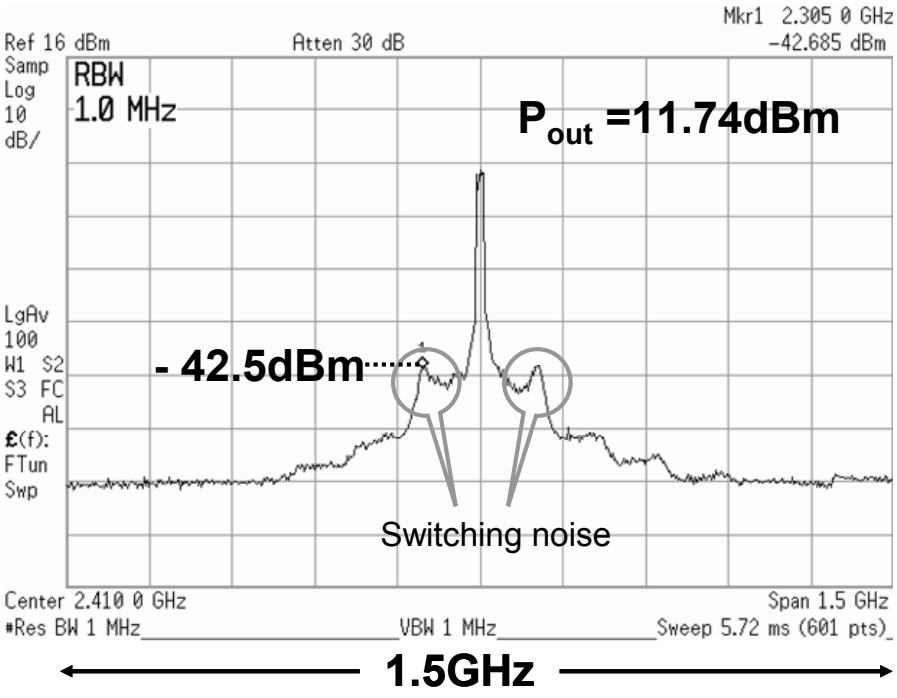


Figure 4.43 Output spectrum for wider band (1.5GHz)

4.6 Conclusions

An integrated polar modulated power amplifier for 20MHz RF bandwidth has been presented. The supply modulator of the polar amplifier has a much larger bandwidth than previously reported in literature while achieving a peak efficiency of 87.5%. At 10dB back-off the efficiency is more than 40%. The topology of the modulator is a parallel AB and D amplifier. The class AB amplifier has a cascoded nested miller topology which allows the switching ripple to be as low as $4.3mV_{rms}$ at a switching frequency of 118MHz. The polar modulated PA satisfies the bandwidth and linearity requirement of the IEEE 802.11g WLAN signal. Operating at 2.41GHz, it delivers an average output power of 11.75dBm with an average PAE of 13.1% for the WLAN signal, including all losses in the passive components of the matching network and balun. The ripple is less than -42.5dBm/MHz in the output spectrum, satisfying the spurious emission requirements.

References

[1] T. Kwak, M. Lee, and G. Cho, "A 2W Hybrid Switching Amplitude Modulator for EDGE Polar Transmitter", *ISSCC Dig. Tech. Papers,* pp. 518-519, February 2007

[2] J. Kitchen, W. Chu, I. Deligoz, S. Kiaei, and B. Bakkaloglu, "Combined Linear and Δ-Modulated Switched Mode PA Supply Modulator for Polar Transmitters", *ISSCC Dig. Tech. Papers*, pp. 82-83, February 2007

[3] P. Reynaert and M. Steyaert, "A 1.75-GHz Polar Modulated CMOS RF Power Amplifier for GSM-EDGE", *IEEE Journal of Solid-State Circuits*, pp. 2598-2608, December 2005

[4] W.Y. Chu, B. Bakkaloglu, and S. Kiaei, "A 10MHz-Bandwidth 2mV-Ripple PA-Supply Regulator for CDMA Transmitters", *ISSCC Dig. Tech. Papers*, pp. 448-449, February 2008

[5] F. Wang, D.F. Kimball, D.Y. Lie, P.M. Asbeck and L.E. Larson, "A Monolithic High-Efficiency 2.4-GHz 20-dBm SiGe BiCMOS Envelope-Tracking OFDM Power Amplifier", *IEEE Journal of Solid-State Circuits*, pp. 1271-1281, June 2007

[6] F. Wang, J.D. Dopp, A.H. Yang, D.Y. Lie, P. M. Asbeck and L. E. Larson, "An Improved Power-Added Efficiency 19-dBm Hybrid Envelope Elimination and Restoration Power Amplifier for 802.11g WLAN Applications", *IEEE Transactions on Microwave Theory and Techniques*, Vol. 54, pp. 4086-4099, December 2006

[7] R. Shrestha, R.A.R van der Zee, A.J.M. de Graauw, and B. Nauta, "A Wideband Supply Modulator for 20MHz RF Bandwidth Polar PAs in 65nm CMOS", *IEEE Journal of Solid-State Circuits,* pp. 1272-1280, April 2009

[8] R. Shrestha, R.A.R van der Zee, A.J.M. de Graauw, and B. Nauta, "A Wideband Supply Modulator for 20MHz RF Bandwidth Polar PAs in 65nm CMOS", *IEEE Symposium on VLSI circuits Dig. Tech. Papers,* pp. 92-93, June 2008

[9] P. Kenington, "High-Linearity RF Amplifier Design", Artech House, 2000

[10] P. Alinikula, K. Choi, and S.I. Long, "Design of Class E Power Amplifier with Nonlinear Parasitic Output Capacitance", *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, Vol. 46, pp.114-119, February 1999

[11] ProMOST by Chip Design Works; (online): www.chipdesignworks.com

[12] R.A.R. van der Zee and A.J.M. van Tujil, "A power-efficient audio amplifier combining switching and linear techniques", *IEEE Journal of Solid-State Circuits*, pp.985-991, July 1999

[13] IEEE P802.11g/D8.2, "Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) specifications: Further Higher Data Rate Extension in the 2.4 GHz Band", April 2003

[14] Advance Design System technical notes, "WLAN Wireless Test Benches", September 2004

[15] R. Hogervorst, J.P. Tero, R.G.H. Eschauzier, and J.H. Huijsing, "A compact power-efficient 3 V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries", *IEEE Journal of Solid-State Circuits*, pp.1505-1513, December 1994

[16] B.K. Ahuja, "An Improved Frequency Compensation Technique for CMOS Operational Amplifier", *IEEE Journal of Solid-State Circuits,* VOL. 18, pp. 629-633, December 1983

[17] H. Aminzadeh, and R. Lotfi, "On the Power Efficiency of Cascode Compensation over Miller Compensation in Two-Stage Operational Amplifiers", *Journal of Circuits, Systems and Computers (JCSC)*, Vol. 16, No. 6, February 2008

[18] N.O. Sokal and A. D. Sokal, "Class E- A new class of high-efficiency tuned single-ended switching power amplifiers", *IEEE Journal of Solid-State Circuits*, pp. 168-176, June 1975

[19] K. Tsai and P.R. Gray, "A 1.9-GHz, 1-W CMOS Class-E Power Amplifier for Wireless Communications", *IEEE J Solid-State Circuits*, pp.962-970, July 1999

[20] A. Grebennikov, "Load network design techniques for class-E RF and microwave amplifiers", *High Frequency Electronics*, pp.18-32, July 2004

[21] W. Bakalski, W. Simburger, H. Knapp, and A.L. Scholtz, "Lumped and Distributed Lattice-type LC-Baluns", in *Proceedings of IEEE International Microwave Symposium*, Seattle, June 2002

[22] R. Chang, D. Weber, M. Lee, D. Su, K. Vleugels, and S. Wong, "A fully integrated RF Front-end with Independent RX/TX Matching and +20dBm Output Power for WLAN Applications", *ISSCC Dig. Tech. Papers*, pp. 564-565, February 2007

[23] A Mazzanti, L. Larcher, and R. Brama, "Analysis of Reliability and Power Efficiency in Cascode class-E PAs", *IEEE Journal of Solid-State Circuits*, pp1222-1229, May 2006

Chapter 5

Conclusions

5.1 Summary and Conclusions

Modern wireless standards use *spectrally efficient* complex modulation schemes and multiple carriers. The modulated RF signal in such systems has a variable envelope with high peak to average power ratio (PAPR) thus requiring linear amplification in the transmitter path. However, linear amplifiers suffer from poor efficiency. On the other hand, there is an increased trend to use wireless transceiver terminals that support an increasing number of different radio standards. A dream is to have a software-defined radio. Furthermore, in order to overcome the *spectrum scarcity* problem, dynamic spectrum access with cognitive radio technology is a very promising approach. In such applications a flexible or reconfigurable hardware platform is needed to allow for a flexible choice of radio frequency. Traditional hardware cannot handle these requirements. This thesis covers solutions to these two problems: (a) a transmitter power efficiency problem amplifying signals with a large PAPR and (b) a lack of flexible RF front-ends to choose an arbitrary RF transmitter frequency. The scope is limited to the RF front-end of the transmitter.

In *chapter 2*, linearity, efficiency and flexibility issues in RF power amplifiers were discussed. To design a power amplifier for digital wireless communication standards, the understanding of the properties of a complex digital modulated signal is necessary in order to optimize the power amplifier's performance in terms of both linearity and efficiency. There are different ways to measure the linearity and the efficiency. Spectral mask, EVM, ACPR, NPR measurements are used to specify the linearity of the transmitter. Similarly, drain efficiency, power added efficiency and average efficiency are used to measure the efficiency performance. A trade-off between linearity and efficiency always exist in stand-alone classic power amplifiers. Linear mode PAs like class-A and class-AB are good for linearity and switch mode PAs like class-E and class-F are good for efficiency. Doherty, LINC, Envelop tracking and Polar Modulation

techniques are known to enhance the efficiency of the power amplifiers, overcoming that trade-off. The second part of this thesis (chapter 4) is dedicated to the polar modulation technique.

No matter which kind of amplifier is used, filters at the output are considered inevitable to suppress the harmonic products generated by non-linearities. The consequence of the presence of fixed frequency filters is that the resulting transmitter hardware is inflexible.

In *chapter 3*, a polyphase multipath technique was implemented with the aim to cancel harmonics and sidebands generated by a non-linear circuit so that there is no need for the fixed frequency output filter. The basic idea is to divide a nonlinear circuit into *n* equal smaller pieces, and apply an equal but opposite phase shift before and after each nonlinear circuit. The phase of the fundamental component is identical for all the paths, but the phases of harmonics are different for each path. With the proper choice of the phase shift the higher order harmonics are cancelled, while the fundamental components add up in phase.

Using this technique, a highly flexible power upconverter was realized in 0.13μm CMOS as a proof of concept. Operating at an arbitrary transmit frequency between DC and 2.4GHz, the output spectrum is clean up to the 17th harmonic of the LO (18-path mode) or 5-th harmonic of the LO (6-path mode) by using a polyphase multipath technique in combination with an LO with 1/3 duty cycle. The unwanted harmonics and sidebands are lower than -40dBc. This work shows that by using polyphase multipath circuit techniques the requirements of filters can be relaxed or completely eliminated, enabling a flexible radio architecture. Furthermore, the power upconverter uses only digital circuits and switched transconductor mixers, making the design suitable for future Software Defined Radio architectures in CMOS.

In *chapter 4*, the details of challenges and prototype implementation of a polar modulated power amplifier, which have the potential to enhance the efficiency while achieving sufficient linearity, were described. In this architecture a phase modulated signal with constant envelope is amplified by a non-linear PA and the amplitude information is restored via its power supply modulation. Key problems for the implementation of polar modulated power amplifiers are bandwidth of the supply modulator, differential delay between the envelope and phase paths, switching noise of the supply modulator, feed-through in the RF PA and nonlinear parasitic output capacitance. Several techniques to overcome those problems are presented. Furthermore this chapter provides a concrete design method for polar power amplifiers in detail.

The key building block of a polar amplifier is the supply modulator. State-of-the-art implementations of supply modulators are reported only for standards with at most a few MHz of signal bandwidth due to the strong requirements for large bandwidth, high efficiency and low-switching ripple. We presented a supply modulator, consisting of a 3-stage cascaded nested Miller compensated linear amplifier and a class D switching amplifier, that can satisfy these requirements. Further in the chapter, the system level

design choices and optimization techniques of the supply modulator for power dissipation and switching residue were presented.

The demonstrator chip of an integrated polar modulated power amplifier for 20MHz RF bandwidth was fabricated in 65nm CMOS. The polar modulated PA satisfies the bandwidth and linearity requirement of the IEEE 802.11g WLAN signal. Operating at 2.41GHz, it delivers an average output power of 11.75dBm with an average PAE of 13.1% for the WLAN signal, including all losses in the passive components of the matching network and balun. We believe that the efficiency can be further improved with a better class-E power amplifier design. The ripple is less than -42.5dBm/MHz in the output spectrum, satisfying the spurious emission requirements. This work shows that, even for the signal with large RF bandwidth, the linearity and other requirements like switching noise are possible to satisfy in the polar amplifier architecture. The supply modulator of the polar amplifier has a much larger bandwidth than previously reported in literature while achieving a peak efficiency of 87.5%.

5.2 Original Contributions

- The efficiency optimization strategy for the design of a supply modulator consisting of linear and switching amplifiers.

- The introduction of the concrete design method for polar modulated power amplifiers in detail for the first time.

- The proposal for a three-stage cascoded nested miller compensated amplifier and a class-D switching amplifier combination to increase bandwidth of a supply modulator and reduce switching ripple. The design of the supply modulator that has a much larger bandwidth than previously reported in literature.

- Realization of the integrated polar modulated power amplifier in 65nm CMOS and laminate.

- The analysis and elaboration of challenges of power modulated power amplifiers through analytical equations and/or simulations

- Realization of a wideband and flexible power upconverter that uses no dedicated filters but only digital blocks and switched transconductor mixers using a polyphase multipath technique

- The introduction of 1/3 duty cycle technique to cancel a problematic 3rd harmonic of LO which can not be cancelled with the polyphase multipath techqniue

5.3 Recommendations for Future Work

The performance of the wideband power upconverter and the polar modulated power amplifier that were presented can be improved. In the following discussion some recommendations are presented.

Wideband Filter-less Power Upconverter for Software-defined Radios

Power consumption of the multiphase signal generation circuit in the current implementation can be reduced. One main reason for higher power consumption is the use of current mode logic circuits for multiphase signal generation that are pushed for high operating frequency with high bias currents. By using standard logic gates or other smarter clock generation architectures, the power consumption can be reduced significantly. Furthermore, newer CMOS technology will also help to reduce the power consumption.

The phase shifter before the nonlinear circuit is a missing piece of jigsaw to enable the design of a complete wideband and flexible transmitter front-end for SDR using the polyphase multipath technique. In a DSP intensive radio transmitter, digital signal processing techniques can be exploited to realize those phase shifters. Therefore, a good solution could be to use a DSP followed by multiple DACs to generate multi-phase baseband signals. Another solution is to upconvert the baseband signal to the intermediate frequency by using multi-phase carriers. The requirement in this case is that the upconverted signal at the intermediate frequency should be sufficiently clean.

Polar Modulated Power Amplifier

The efficiency of the polar modulated PA can be further improved at low envelop power. This can be done, for example, by using multiple power switches in parallel instead of one big switch for the class-E power amplifier such that only the part of the final switch is activated for low output power. The driver of the PA and class D amplifier can also be designed in the same way to minimize switching and driving losses at low envelope power. It is worth investigating such a technique to improve the efficiency.

In the current implementation (chapter 4), the feed-through via the drain-source capacitor of the power switch to the output of the final PA (class-E) is the main source of AM-AM and AM-PM distortion at low envelope power. One way to cancel this effect in a differential PA configuration is by adding a cross-coupled capacitor from the gate of one power switch to the drain of the other such that the feed-through current is cancelled by the added capacitor current. Further investigation on this or other technique to improve the linearity is valuable. Any improvement in the linearity can be directly traded for efficiency improvement.

Samenvatting

Moderne standaarden voor draadloze communicatie gebruiken spectraal efficiënte modulatietechnieken en meerdere draaggolven. Het gemoduleerde radiofrequente (RF) signaal in zulke systemen heeft een omhullende die sterk in de tijd varieert, waardoor men is aangewezen op een versterker die voldoende lineair is. De meeste lineaire versterkers, echter, hebben een laag rendement. Naast de complexe modulatietechnieken is er ook een trend naar ontvangers die meerdere radiostandaards tegelijk ondersteunen. Het ideaal is dan om een radio te hebben die helemaal door software wordt definieerd: "software defined radio". Verder is er het probleem van spectrum schaarste. Een veelbelovende techniek om spectrum schaarste het hoofd te bieden is cognitieve radio: een flexibele of reconfigureerbare radio die zelf een beschikbare frequentie zoekt en gebruikt. Standaard radio's kunnen niet aan deze eisen voldoen, en dit proefschrift draagt bij aan de oplossing van deze twee problemen: (a) het lage rendement van zenders voor signalen met een sterk variërende omhullende en (b) het gebrek aan flexibele radio's die een willekeurige zendfrequentie kunnen gebruiken.

In hoofdstuk 2 worden de lineariteit, het rendement en de flexibiliteit van RF vermogensversterkers bekeken. Kennis van complexe digitale modulatietechnieken is noodzakelijk om een RF vermogensversterker te ontwerpen die zowel lineair als energiezuinig is, en in de praktijk moet er altijd een afweging tussen deze twee eigenschappen gemaakt worden. Klasse A en klasse AB versterkers hebben een goede lineariteit, en geschakelde versterkers zoals klasse E en klasse F halen een hoog rendement. Die afweging hoeft in mindere mate gemaakt te worden bij Doherty versterkers, LINC versterkers, en polaire versterkers. Polaire versterkers zijn versterkers met een voeding die de omhullende van het RF signaal volgt, en deze zijn het onderwerp van het tweede deel van dit proefschrift (hoofdstuk 4).

Echter, ongeacht welk type versterker men gebruikt, de uitgang moet altijd gefilterd worden om de harmonischen te filteren die zijn ontstaan door niet-lineariteiten. Normaal wordt hiervoor een filter met een vaste frequentie gebruikt, maar dat heeft tot gevolg dat de radio niet meer flexibel is.

In hoofdstuk 3 wordt een polyfase techniek met meerdere paden gerealiseerd met het doel om harmonischen en zijbanden te onderdrukken die ontstaan door niet-lineariteiten. Hierdoor is er idealiter geen filter aan de uitgang meer nodig. Het idee is om een niet-lineair circuit onder te verdelen in de som van n kleinere delen. Het in- en uitgangssignaal van elk deel wordt (omgekeerd) in fase verschoven, waardoor de fase van de grondtoon

van elk deel gelijk is, maar de fase van de harmonischen verschilt. Door de fasedraaiingen goed te kiezen, tellen de basiscomponenten van alle paden op, terwijl de harmonischen elkaar opheffen.

Met behulp van deze techniek is een flexibele vermogensmixer gerealiseerd in 0.13µm CMOS. Deze kan werken met een willekeurige zendfrequentie tussen DC en 2.4GHz, en door het gebruik van de polyfase techniek en een oscillatorsignaal met een duty cycle van 1/3e is het uitgangsspectrum schoon tot de 18e harmonische van het oscillatorsignaal in 18-pad mode en tot de 6e harmonische in 6-pad mode. De ongewenste harmonischen en zijbanden liggen meer dan 40dB onder de draaggolf. De uitgangsfilters hoeven hierdoor aan aanzienlijk lagere specificaties te voldoen of kunnen zelfs worden weggelaten, waardoor het gemakkelijker wordt om flexibele radio's te realiseren. De vermogensmixer gebruikt bovendien alleen maar digitale circuits en geschakelde transconductanties, zodat hij goed schaalbaar is naar toekomstige CMOS processen.

Hoofdstuk 4 richt zich op het ontwerp en de realisatie van een polaire versterker. In deze architectuur wordt een fase-gemoduleerd signaal met constante amplitude versterkt door een niet-lineaire RF vermogensversterker, waarbij de amplitude-informatie wordt overgebracht door de voedingsspanning van deze versterker te variëren. De grootste uitdagingen zijn de bandbreedte en het schakelresidu van de voedingsspanning modulator, het verschil in looptijd tussen fase- en amplitudepad, en de voedingsspanningsafhankelijke fasedraaiing en niet-lineaire uitgangscapaciteit in de RF versterker. Concrete oplossingen voor deze problemen en een gedetailleerde ontwerpmethode worden gepresenteerd.

Een essentieel onderdeel van een polaire versterker is de voedingsspanning modulator. Door de strenge eisen aan bandbreedte, rendement en schakelresidu, zijn de in de literatuur gerapporteerde modulatoren alleen geschikt voor radiostandaarden met slechts een paar MHz bandbreedte. Het blijkt mogelijk een voedingsspanning modulator met een grotere bandbreedte te realiseren die toch aan alle andere eisen voldoet. Naast de realisatie komen ook de systeemkeuzes die daarvoor gemaakt worden en de optimalisatietechnieken in dit hoofdstuk aan bod.

Een demonstratiechip van een geïntegreerde polaire versterker met 20MHz RF bandbreedte werd gefabriceerd in 65nm CMOS. De versterker voldoet aan de bandbreedte- en lineairiteitseisen van het IEEE 801.11g WLAN signaal. Op 2.41GHz levert de versterker een gemiddeld uitgangsvermogen van 11.75 dBm met een gemiddelde PAE van 13.1% voor het WLAN signaal, inclusief alle verliezen in de passieve componenten van het matching netwerk en de balun. Het schakelresidu aan de uitgang ligt onder de -42.5 dBm/MHz, waardoor deze versterker voldoet aan de eisen van ongewenste emmissie. Dit werk toont aan dat polaire versterkers ook te realiseren zijn voor grotere RF bandbreedtes. De gebruikte voedinsspanning modulator heeft een bandbreedte die veel groter is dan tot nu toe gepubliceerd, en heeft een maximum rendement van 87.5%.

Appendix A

Canceling Harmonics with 3-paths

In this appendix, the mathematical illustration that shows the cancellation of 2nd, 3rd etc harmonics is given for the 3-path polyphase circuit.

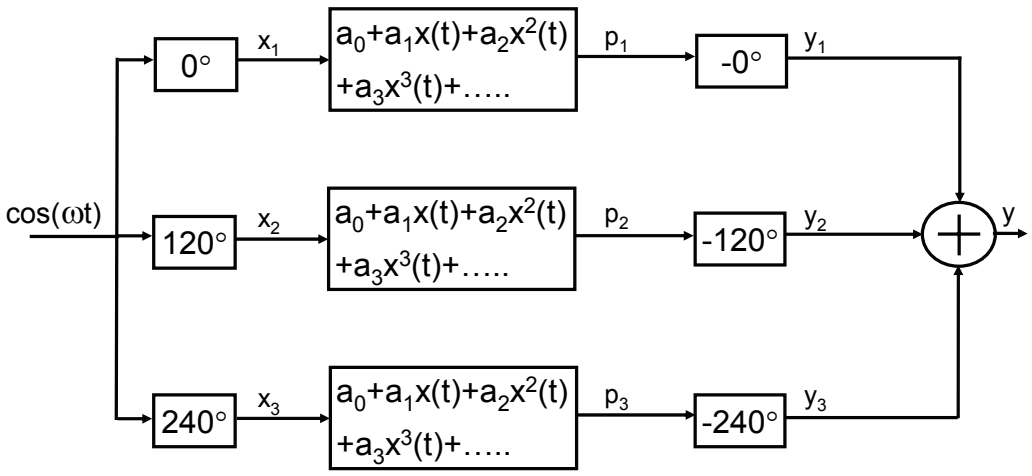


Figure A.1. Canceling the harmonics of order 2nd, 3rd, 5th, 6th, 8th and so on with 3 paths

If the input signal x(t)=Asin(ωt) is applied to the 3 path system in Figure A.1, then the signal at x_o, x_1 and x_2 will be

$$x_1 = A\sin(\omega t)$$
$$x_2 = A\sin(\omega t + 120^\circ)$$
$$x_3 = A\sin(\omega t + 240^\circ)$$

Then as shown in equation 3.3 the output of the non-linear system at the i^{th} path will be

$$p_1 = \left(a_0 + \frac{a_2 A^2}{2}\right) + \left(a_1 A + \frac{3a_3 A^3}{4}\right)\cos(\omega t) + \frac{a_2 A^2}{2}\cos(2\omega t) + \frac{a_3 A^3}{4}\cos(3\omega t) + ...$$

$$p_2 = \left(a_0 + \frac{a_2 A^2}{2}\right) + \left(a_1 A + \frac{3a_3 A^3}{4}\right)\cos(\omega t + 120) + \frac{a_2 A^2}{2}\cos(2\omega t + 240)$$

$$+ \frac{a_3 A^3}{4}\cos(3\omega t + 360) + ...$$

$$p_3 = \left(a_0 + \frac{a_2 A^2}{2}\right) + \left(a_1 A + \frac{3a_3 A^3}{4}\right)\cos(\omega t + 240) + \frac{a_2 A^2}{2}\cos(2\omega t + 480)$$

$$+ \frac{a_3 A^3}{4}\cos(3\omega t + 720) + ...$$

The phase shifter after the non-linear component in Figure A.1 modifies the phases of the signal in each path to

$$y_1 = \left(a_0 + \frac{a_2 A^2}{2}\right) + \left(a_1 A + \frac{3a_3 A^3}{4}\right)\cos(\omega t) + \frac{a_2 A^2}{2}\cos(2\omega t) + \frac{a_3 A^3}{4}\cos(3\omega t) + ...$$

$$y_2 = \left(a_0 + \frac{a_2 A^2}{2}\right) + \left(a_1 A + \frac{3a_3 A^3}{4}\right)\cos(\omega t) + \frac{a_2 A^2}{2}\cos(2\omega t + 120) + \frac{a_3 A^3}{4}\cos(3\omega t + 240) + ...$$

$$y_3 = \left(a_0 + \frac{a_2 A^2}{2}\right) + \left(a_1 A + \frac{3a_3 A^3}{4}\right)\cos(\omega t) + \frac{a_2 A^2}{2}\cos(2\omega t + 240) + \frac{a_3 A^3}{4}\cos(3\omega t + 120) + ...$$

The summation of these signals can be written as

$$y = y1 + y2 + y3 = \left(a_0 + \frac{a_2 A^2}{2}\right) + \left(a_1 A + \frac{3a_3 A^3}{4}\right)\cos(\omega t) + \frac{a_4 A^4}{4}\cos(4\omega t) + ... \qquad \text{A.1}$$

Because,

$$\cos 2\omega t + \cos(2\omega t + 120) + \cos(2\omega t + 240) = \sum_{i=1}^{3}\cos(2\omega t + (i-1)\varphi) = 0$$

$$\cos 3\omega t + \cos(3\omega t + 240) + \cos(2\omega t + 120) = \sum_{i=1}^{3}\cos(3\omega t + 2(i-1)\varphi) = 0$$

and so on.

The harmonics of the order 2nd, 3rd, 5th and so on from all the paths create a balanced structure. So, the resultant of these harmonics will be zero at the output as shown in equation A.1.

List of Publications

1. **R. Shrestha**, R.A.R van der Zee, A.J.M. de Graauw, and B. Nauta, “A Wideband Supply Modulator for 20MHz RF Bandwidth Polar PAs in 65nm CMOS”, *IEEE Journal of Solid-State Circuits,* pp. 1272-1280, April 2009

2. **R. Shrestha**, E. Mensink, E.A.M. Klumperink, G.J.M. Wienk, and B. Nauta, "A Polyphase Multipath Technique for software-defined radio transmitters", *IEEE Journal of Solid State Circuits*, Vol. 41, pp. 2681-2692, December 2006

3. E.A.M. Klumperink, **R. Shrestha**, E. Mensink, **X. Gao** and B. Nauta, “Multipath Polyphase Circuits and Multi-Phase Clock Generation”, invited lecture at the *Caltech RF/Microwave seminar*, Pasadena, February 2009

4. **R. Shrestha**, R.A.R van der Zee, A.J.M. de Graauw, and B. Nauta, “A Wideband Supply Modulator for 20MHz RF Bandwidth Polar PAs in 65nm CMOS”, *IEEE Symposium on VLSI circuits Dig. Tech. Papers,* pp. 92-93, June 2008

5. E.A.M. Klumperink, **R. Shrestha**, E. Mensink, **X. Gao** and B. Nauta, “Multipath Polyphase Circuits for Cognitive Radio Transmitters”, invited lecture at the *IEEE MTT-S International Microwave Symposium (IMS) 2008 workshop “WMB: Enabling Technologies for Wireless Transceivers Beyond-3G”*, June 2008

6. E.A.M. Klumperink, **R. Shrestha**, E. Mensink, V.J. Arkesteijn, and B. Nauta, “Polyphase Multipath Radio Circuits for Dynamic Spectrum Access”, *IEEE Communications Magazine*, Vol. 45, Issue 5, pp. 104 – 112, May 2007

7. E.A.M.Klumperink, **R. Shrestha**, E. Mensink, G. J. M. Wienk, Z. Ru, and B.Nauta, "Multipath Polyphase Circuits and their Application to Radio Transceivers", Proceedings of the 2007 *IEEE International Symposium on Circuits and Systems (Invited paper)*, 27-30 May 2007, New Orleans, USA, pp. 273-276, May 2007

8. **R. Shrestha**, E. Mensink, E.A.M. Klumperink, G.J.M. Wienk, and B. Nauta, "A Wideband Flexible Power Upconverter for Software Defined Radios", *Proceedings of the 17th Annual Workshop on Circuits, Systems and Signal Processing, ProRISC*, 23-24, pp.85-89, November 2006

9. **R. Shrestha**, E. Mensink, E.A.M Klumperink, G.J.M. Wienk B. Nauta "A Multipath Technique for Canceling Harmonics and Sidebands in a Wideband Power Upconverter" *International Solid State Circuits Conference* (*ISSCC) Dig. Tech. Papers*, pp. 452-453, February 2006

Acknowledgements

Writing this part of the thesis is emotional as I start to remember many people who directly or indirectly supported, assisted and encouraged me in all those years in the preparation and completion of this thesis.

First and foremost, I would like to express my deepest gratitude and endless thanks to my promotor, Bram Nauta, whose continuous encouragements and support I will never forget. His invaluable advice, thoughtful guidance and great ideas were a constant source of motivation that inspired and enriched my growth as a student and a researcher.

I am deeply indebted to my assistant promoter Ronan van der Zee for his supervision, advice and crucial contribution. Without his constant encouragements and suggestions, this thesis would not have been completed. I am grateful to you in every possible way. Ronan, I also very much enjoyed our every discussions on the project which made me mature scientifically. I would also like to thank you for very constructive comments which made this thesis more precise.

I gratefully thank Anton de Graauw of NXP semiconductors for invaluable suggestions and comments. Especial thanks for facilitating the fabrication and assembly of the laminate module.

I owe my deepest gratitude to Eric Klumperink for his advice and guidance since my Master study. You were always inspirational and I learned a lot from you about IC design.

I am very grateful to Henk de Vries for providing excellent support during measurements in the lab and to Gerard Wienk for his assistance in layout and CAD tools. I always found them so kind and friendly.

My sincere appreciation goes to Gerdien Lammers for providing all the necessary administrative support. You are so kind and simply the best secretary I have ever worked with. I am also thankful to Annemiek Janssen for her kindness and suggestions in administrative work. I thank Frederik Reenders for helping to solve the PC related problems.

I am very grateful to all members of the graduation committee for taking time to read this dissertation and for their approval and comments.

It is my privilege to work in the Integrated Circuit Design chair, which is full with very enthusiastic and helpful people around that made me feel like family with so much fun. Many thanks go in particular to my officemates Paul Veldhorst, Eric Hoekstra, and Arnoud van der Wel for making very enjoyable atmosphere at office. Paul, especial thanks to you for helping me in so many things, from finding a new house to providing many tips and tricks for 'survival' in the Netherlands. I am indebted to my colleagues Stephan Blaakmeer, Vincent Arkesteijn, Simon Louwsma, Daniel Schinkel, Eisse Mensink, Zhiyu Ru and Wei Cheng for their very cheerful friendship and memorable time. I would like to express my sincere thanks to Paul Geraedts, Seyed Kasra Garakoui, Mustafa Acar, Saqib Subhan, Jan Rutger Schrader and all the members of IC design group and Semiconductor components group for making those years very enjoyable.

Nepalese community in Enschede played an important role in making me feel like home. I am particularly thankful to the family of Dhruba and Sangita Shrestha, and Manfred and Reena Pulles for their hospitality, kindness and delicious Nepalese food. I would also like to thank Neeva Shrestha and Sandhya Shrestha for their care and kindness to my family. My special thanks to Ravi Khadka, Ajay Bhakta Mathema, Mohan Raj Adhikari for making those years more homely and enjoyable.

I would like to express my most special thanks to my beloved family members. My dearest parents always gave me immense support, encouragements and inspiration that kept me moving in difficult times. My aunts cared me so much from the childhood and always sent me their prayers wholeheartedly. This thesis is dedicated to my parents and aunts. I am greatly indebted to my brothers, sisters and sister-in-law for their unconditional support, love and care.

Words are simply not enough to express my appreciation to my wife Gehini for her love, dedication, support, and for taking care of our little son, Ruben, in difficult times. Dear, you always make sure that I get enough time to spend in the thesis and without your great understanding this thesis would not have completed. As to my little boy, Ruben, my love for you is beyond words. He brought so much happiness in our life.

About the Author

Rameswor Shrestha was born in Kavre, Nepal, in 1976. He received the B.E. degree (*with distinction*) from the Kathmandu University, Nepal, in 2000 and the M.Sc. degree (*cum laude*) from the University of Twente, The Netherlands, in 2004, both in electrical engineering. He is a Ph.D. candidate at the University of Twente and currently working as a Research Scientist at the Mixed-Signal Circuits and Systems group of NXP Research, Eindhoven, The Netherlands. His research interests include power management circuits, supply modulators, and RF power amplifiers.